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Distance-Learning Tools for Digital Design and Test Issues

Artur Jutman, Margus Kruus, Alexander Sudnitson, Raimund Ubar
Tallinn Technical University, Raja 15, 12618 Tallinn, Estonia
Tel. 372 620 2252; Fax: 372 620 2253; {artur,raiub}@pld.ttu.ee, {kruus,alsu}@cc.ttu.ee

Abstract. *The paper presents a new teaching conception for distance-learning based on using of so called "living pictures". The field considered covers computer engineering, switching and automata theories, and more specifically, design and test of digital circuits and systems. A set of tools ("interactive modules") is offered which support different stages of the learning process: class teaching, individual home training, self-testing, and examination as well.*
Key words. Distance-learning, Applets, Automata decomposition, Register-transfer level, test

1. Introduction

The electronics sector now represents around 10% of world trade [1], which can largely be attributed to the engineering and technological advances in the Integrated Circuit (IC) industries. To cope with today's demands in the very rapidly developing electronics industry, the engineering curricula and teaching technologies must be constantly updated. The more complex are getting electronics systems, the more important will be the problems of test and design for testability because of the very high cost of testing electronic products. Design and test are no longer separate issues. Entering into the System-on-Chip (SOC) era means that test must now become an integral part of the VLSI and system design courses.

In this paper, a conception is presented how to improve the skills of students to be educated for hardware and SOC design in test related topics. We present a learning method based on using so-called *living pictures* [2,3]. The method presented deals with the goal, to put interactive teaching modules to the Internet that can be used in a lecture as well as for individual self-studies [2]. They can be accessed independent of time and place. On one hand, teachers can demonstrate different examples and procedures of test related topics using computer simulated living pictures during their lessons. On the other hand, students can use the same simulations on their home computer, if the living pictures are available on the Internet. The core of the teaching concept presented are some JAVA-applets (interactive modules) running on any browser connected to the Internet.

The paper is structured as follows. In Section 2 we describe the applets developed for teaching some theoretical problems of automata theory. Section 3 presents the applet for learning logic level test problems. Section 4 is devoted to the register-transfer (RT) level simulation. In Section 5 we shortly describe a tool-set for hands-on teaching logic level design and test, and, finally in Section 6 we draw some conclusions.

2. Applets for automata decomposition

This part of work focuses on particular but comprehensive problem of decomposition of finite automata (finite state machine). Theoretical background of our system is the automata decomposition theory, which uses partition pair algebra proposed in [4]. The importance of this theory lies in the fact that it provides a direct link between algebraic relationships and physical realizations of finite state machines. The mathematical foundation of this theory rest on an algebraization of the concept of "information" in a machine and supply the algebraic formalism necessary to study problems about the flow of this information in machines as they operate. It falls squarely in the interdisciplinary area of applied algebra, which is a part of engineering mathematics. We are concerned with solving complex combinatorial tasks arising from the process of design.

In this part of the distance-learning tool set, different applets for studying the basics of the decomposition theory of automata have been developed [5]. The applet on construction of an automata network allows experimenting with decomposition of automata. Different partitions can be chosen to decompose the given sequential machine to meet different design restrictions.

The developed set of applets can be used for teaching the basics of automata theory. The teacher can use the applet during the lecture explaining the basics of the topic. On the other hand, the applet can be used during the exam for giving some tasks to students. Students can use the same applet for training purposes.

3. Applet for learning logic level test

This applet (Fig.1) was developed to study the basic problems in the field of logic level testing, especially, in fault simulation, test generation, and fault location [6].

From the list of predefined circuits by *schematics menu*, a simple circuit under test (CUT) can be chosen. The *mode menu* tells the applet what is to be done – automated or manual test vector insertion, manual test vector generation, fault simulation or fault diagnosis (two possible modes: sequential and combinational diagnosis).

In *test generation mode* we choose a target fault in the circuit, and create manually step by step proper activated paths in the circuit with the goal to find a pattern which tests the fault. We have to activate the fault at its site, and to propagate the error signal to the output by clicking the needed signal values on the lines in the CUT. The colours on lines help to understand the current status of the task: activated faults and activated paths are marked by red and green

lines, the inconsistencies of the signal values are highlighted by blue colour. The faults detected by the generated test pattern are displayed in the form of fault table.
In *fault simulation mode*, a fault table is generated and shown for all the test patterns generated by the given moment.
In *fault diagnosis mode* we need first, to create a fault table by running the fault simulator for a set of previously generated test patterns. Entering into the diagnosis mode will insert a random fault into the circuit. The following diagnosis strategies chosen from menu can be investigated: combinational and sequential diagnosis. For learning the

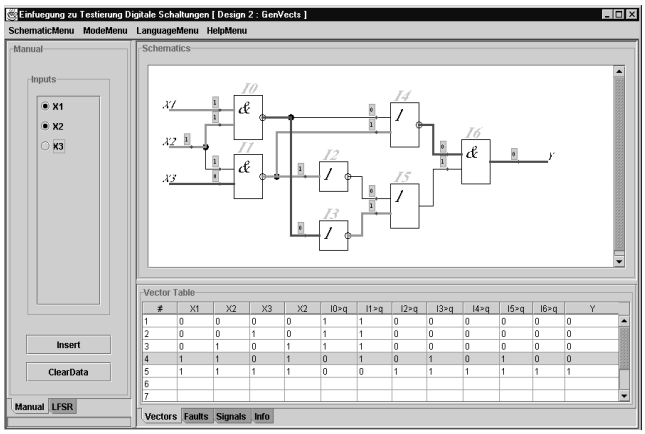

Figure 1. "Living picture" as a Java applet

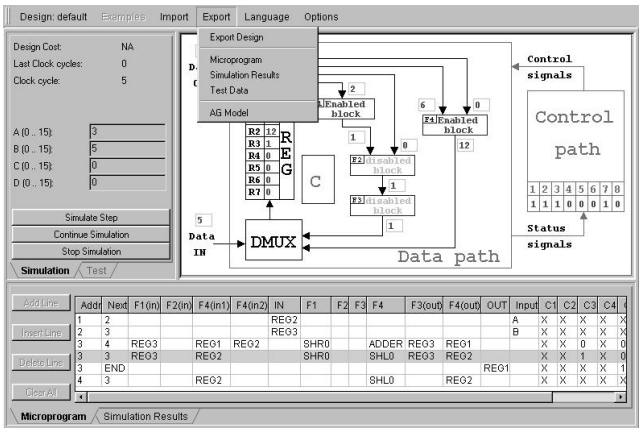

Figure 2. Java-applet for RT-level design and test

combinational diagnostic strategy, a single vector or a subset of vectors can be selected and applied to the erroneous circuit (by imitating test experiments). The applet shows the results of testing, and displays also the subset of suspected faults. To improve the diagnostic resolution, additional test vector(s) may be generated and used in the repeated test experiment. Sequential diagnosis is based on the guided probing strategy. A test pattern is applied and the expected behavior of the circuit is displayed. By clicking on the connection boxes the real values of signals of the faulty circuit can be measured.

The main didactic point in learning the diagnostic strategies is to try to find the fault by as few test patterns or by as few measurements as possible. A competition between students can be carried out which makes the "play" with the applet even more exciting. The applet is easy to use. Students can insert different faults, watch how the faults change the circuit's behavior. They can study how the test patterns should be generated to detect a given fault, or how the faults can be localized by a given test.

4. RT-level design and test applet

The register transfer level design and test applet (Fig.2) allows to solve and illustrate many problems related to RT-level control intensive digital design together with test [5,6].
The range of problems includes (but is not limited to):

- Design of data path and a microprogram (control path) on the RT-level
- Investigation of tradeoffs between the speed and hardware cost in the system
- RT level simulation
- Fault simulation and test coverage evaluation
- Test generation
- Design for testability and BIST

In this work different data-path architectures can be chosen – M-automaton, sequential and parallel IM automata. Each functional unit of the data-path network has a list of micro-operations, which can be optionally selected for the target-implementation. The units are supported by the RT-level and gate-level models of the microoperations. The RT-level model is needed for high-level simulation while the gate-level model is used for gate-level logic and fault simulation. All the microoperations are labeled by a control signal, which activates the microoperation.

While designing a device (implementing a given algorithm) a student can select the needed microoperations for each unit of the data path from the whole set of pre-designed microoperations. Each microoperation has a gate-level implementation, and the number of gates determines the cost of the microoperation. For each design the student will get also the cost of it in the number of gates. The control path is a microprogrammed controller [7], which implements Mealy final state machine. The controller consists of a microprogram table and an interpreter. The microprogram will be developed by the user. The synthesized system can be simulated on the RT-level to verify the correctness of implemented algorithms.

For test generation no special automatic means will be provided. Either manually generated functional patterns or randomly chosen patterns (test data) can be used. For testing the blocks of the data-path, a special test microprogram can be implemented. The quality of tests can be estimated by gate-level fault simulation.

Fault simulation is carried out at the gate level. The process is controlled by the data in the microprogram table. The target of the fault simulation (a unit or the implemented microoperation in the unit) are selected by a student and then highlighted. The fault simulation data is reported as a fault table.

Two modes of Built-In Self-Test (BIST) architectures are implemented: BILBO (Built-In Logic Block Observer) mode based on using random test pattern generator (TPG) and signature analyzer (SA), or CSTP (Circular Self-Test Path) mode based on using combined TPG/SA scan-path register [8]. Both modes can be implemented in two ways: different settings for each combinational circuit to be tested, or the same setting for all circuits. The aim of a student's work is to find best settings.

5. PC-tools for advanced training test

Traditional VLSI test generation and fault simulation software tools on workstations are both costly and unable to handle large numbers of students simultaneously in educational courses. Low-cost systems for solving a large class of tasks from the test area are missing. For this reason, at TU Tallinn the diagnostic software Turbo-Tester (TT) [6] has been developed.

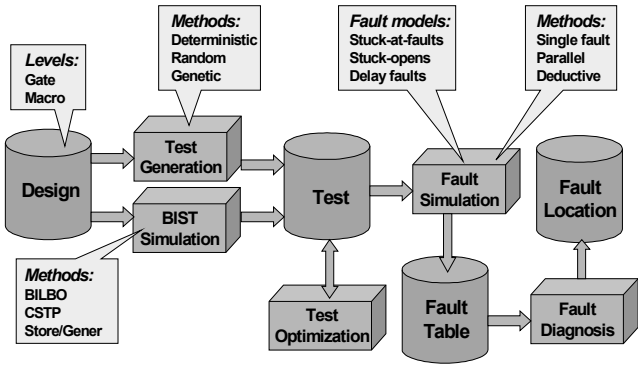

Figure 3. TT diagnostic tool set

After theoretical investigation of the basic test topics described in the previous sections, a laboratory work follows with more complex designs, where the arbitrary available design software (schematic editor as minimum), and the TT diagnostic software is used.

TT (Fig.3) consists of a set of tools for solving different test related tasks by different methods and algorithms: test pattern generation by deterministic, random and genetic algorithms, test program optimization, fault simulation and grading, multi-valued simulation for analyzing dynamic behaviour of circuits, testability analysis and fault diagnosis. The circuit can be modelled at gate- or macro levels which gives a possibility to investigate the complexity issues of different test algorithms. TT can be installed under Windows/NT and Solaris. It can read schematic entries of various CAD tools, e.g. Cadence, Synopsys, Mentor Graphics. Many of the commercially available and in-house test design systems have usually problems with the design interface. Similarly to the Java-based applets, TT tools are accessible over Internet [6].

6. Conclusion

By the use of web-based media we achieve: presentation of course material independent of place and time, individual learning according to the students' own needs, new forms of communication between teachers and students etc. The conception presented allows to improve the skills of students to be educated for electronics design and test related topics. The principal mission of the conception is to inspire students to learn, and to prepare them for developing problem-solving strategies.

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