Study of Real CMOS Defects

name _____

matricul. nr. _____

group _____

register at: *http://www.defsim.com*

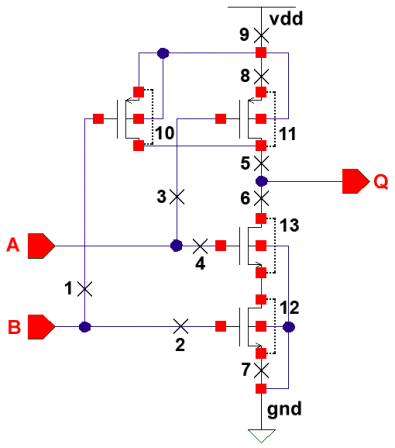
1. Behavior of Open Faults inside a gate

Given circuit: **NA2_o** given defects: _____

1) Manually compose all possible test vectors for all given open defects in *NA2_o* circuit.

2) Check the results in DefSim environment (http://www.defsim.com).

3) Fill-in the table. Analyze the behavior of defects.



BA	Defect 1:	Defect 2:	Defect 3:
00			
01			
10			
11			

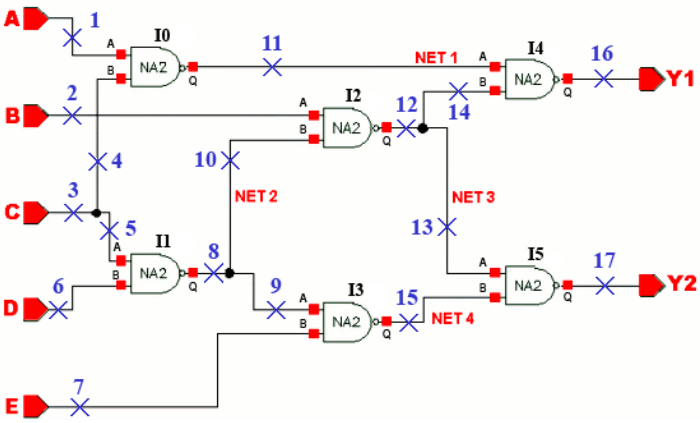
2. Open Faults between the gates : stuck-at-0 or stuck-at-1?

Given circuit: **C17_o** given defects: _____

1) Manually compose two types of test vectors for all given open defects in *C17_o* circuit. Find all possible test patterns for stuck-at-0 (s-a-0) and for stuck-at-1 (s-a-1) fault models.

2) In DefSim environment run exhaustive test for the given defect and check which ones of your vectors detect the defect.

3) Which fault model stuck-at-0 or stuck-at-1 does better describe the defect behavior?



Test no.	Defect 1:		Defect 2:	
	s-a-0	s-a-1	s-a-0	s-a-1
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				

3. Behavior of Short Defects: Wired-AND or Wired-OR?

Given circuit: _____ given defect: _____

1) Manually compose two types of test vectors for a given short defect in a given circuit. Find all possible test patterns for wired-AND and for Wired-OR fault models.

2) In DefSim environment run exhaustive test for the given defect and check which ones of your vectors detect the defect.

No.	Wired-AND	Wired-OR
1		
2		
3		
4		
5		
6		

3) Which fault model Wired-AND or Wired-OR does better describe the defect behavior?

4. Victim-Aggressor fault model – what is stronger input or output?

Given circuit: _____ given defect: _____

1) Manually find all possible test vectors for a given short between circuit's given input and output using Victim-Aggressor fault model. Consider both cases:
   a) when output is aggressor and input is victim
   b) when input is aggressor and output is victim

2) Apply an exhaustive test to the corresponding defective circuit and obtain the fault detection information.

3) Make conclusion about real victim and aggressor.

No.	Input is stronger	Output is stronger
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		

5. Does SAF test detect all real defects in the circuit?

Given circuit: _____

1) In DefSim, generate stuck-at fault (SAF) test for a given circuit.

2) Apply this test to all defects in a given circuit.

3) If there are undetected defects, find additional test patterns (using transistor-level schematic if necessary).

4) Check using DefSim, if your final test set is complete.

Nr.	Test Patterns
1	
2	
3	
4	
5	
6	
7	
8	

6. Defect observability improvement by I_{DDQ} measurement

Given circuit: _____

1) Find undetectable defects in a given circuit using exhaustive test.

2) Activate I_{DDQ} and repeat the measurement. Compare the results.

3) Find the minimum number of test patterns needed to achieve 100% fault coverage for a given circuit. Fill them into the table.

Nr.	Test Patterns
1	
2	
3	
4	
5	