name _____

matricul. nr. _____

group _____

Optimization of Built-in Self-Test

Properties of selected circuits

Circuit	Name	# of inputs	# of outputs
C1			
C2			
C3			

Selected BIST Configuration

TG length _____

SA length _____

1. Broadcasting BIST

Making preliminary experiments

(bist –rand –glen ... –alen ... –optimize 2 –count ... <*circuit*>)

Nr.	Circuit 1		Circuit 2		Circuit 3	
	# of vects	fault cov.	# of vects	fault cov.	# of vects	fault cov.
1						
2						
3						
4						
5						
6						
7						
8						
9						
10						
11						
12						
13						
14						
15						

Selection of the best configuration

Circuit	Configuration 1		Configuration 2		Configuration 3	
	# of vects	# of tested	# of vects	# of tested	# of vects	# of tested
1		/		/		/
2		/		/		/
3		/		/		/
Max/Total	MAX	TOTAL,%	MAX	TOTAL,%	MAX	TOTAL,%
Quality						

Solution Quality Level = $\alpha \cdot Q_{\%} - \beta \cdot Q_V$, where

$Q_{\%}$ is the fault coverage level (FC,%),

Q_V is the test length (No. of vectors)

Choose α and β so, that test length increase by 1000 vectors is justified by 1% of FC gain

2. Hybrid BIST (with reseeding)

(report –progress <*circuit1*>)

Initial vector count *L* _____ Target vector count *L/2* _____

Nr.	Generation of vectors			Vectors to skip
	Seed	Stop	# of vectors	
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				
16				
17				
18				
19				
20				
Total				

Cost_____

(each stored seed costs as much as 50 on-line generated test vectors)

3. Manual LFSR optimization

1. Take a circuit from Lab 1
2. In the applet (http://www.pld.ttu.ee/applets/td/) select initial state and polynomial as you like
3. Generate vectors until you reach 100% FC but not more than 40
4. Identify possible problems with FC caused by selected initial state and polynomial
5. Propose some solutions and apply them
6. Discuss the results with teacher