Design for Testability Work

name _____
matriculation nr. _____
group _____

1. Deterministic ATPG

	Original Design	Observable Circuit I	Observable Circuit II	Controllable Circuit	Testable Circuit I	Testable Circuit II
Number of I/O Pads (inputs+outputs)						
Number of Test Vectors						
Fault Coverage, [%]						
Number of Tested Faults						
Cost						

2. BILBO emulator

TG length _____ SA length _____

	Original Design	Observable Circuit I	Observable Circuit II
Number of I/O Pads (inputs+outputs)			
Number of Test Vectors			
Fault Coverage, [%]			
Number of Tested Faults			
Cost			

TG length _____ SA length _____

	Controllable Circuit	Testable Circuit I	Testable Circuit II
Number of I/O Pads (inputs+outputs)			
Number of Test Vectors			
Fault Coverage, [%]			
Number of Tested Faults			
Cost			

Cost = $\alpha \cdot C_H + \beta \cdot C_V$, where
C_H is the hardware cost (No. of I/O pads),
C_V is the cost of test length (No. of vectors)
Choose α and β so, that one I/O pad had the same cost as 5 test vectors