1. Description of the research proposal

a) Duration of the project and expected total cost

Duration 4 years (2006-2009) with total cost 839 000.- EEK

b) General background

About the importance of the research problem: Today's microelectronics technology provides designers the possibility to integrate a large number of different functional blocks, usually referred as cores, into a single integrated circuit (IC). Such a design style allows designers to reuse previous designs and will lead therefore to shorter time-to-market and reduced cost. Such a system-on-chip (SoC) approach is very attractive from the designers' perspective. Testing of such systems, on the other hand, is a problematic and time consuming task, mainly due to the resulting IC's complexity and the high integration density [1].

According to the International Technology Roadmap for Semiconductors (ITRS), by the end of the decade, SoC, using 50-nm transistors operating below one volt, will grow to 4 billion transistors running at 10 GHz [2]. Such SoCs, based on nanometer-technologies, will most likely suffer from fault effects and new sources of errors that make them unfit for dependable systems, unless a high degree of fault tolerance and error compensation is built into such systems.

As indicated by several authors and the ITRS, nanometer SoCs will most likely not have an economic yield if all transistors must be functional [3]. Furthermore, deep sub-micron technologies will suffer from single event upsets (SEUs) caused by electromagnetic interference and by radioactive particles that trigger non-permanent faults. Finally, the specifically higher strain on materials caused by higher current densities and higher field strength is likely to cause wear-out effect in the field of operation. A design and test technology that may facilitate dependable systems on hardware that is not highly dependable is therefore becoming a must.

A major concern for such multi-billion transistor SoCs is also communication infrastructure, connecting the cores. To prevent the design of the communication architecture from becoming the bottleneck in the design of future SoCs, this communication architecture itself must be compositional and scalable. For that reason the on-chip interconnect will increasingly be implemented as a network-on-chip (NoC), complete with network interfaces, routers, and packet or circuit switching [4], [5]. Testing such systems shares all the problems related to testing modern nanometer SoCs, and introduces also some additional challenges due to the new issues, such as increased long wiring, that is much more vulnerable to timing errors and crosstalk. Therefore, for very large NoCs, additional test strategies, such as those applied in FPGAs should also be included.

Critical overview of previous results: There are two ways to meet the quality constraints of the system. Either to add some form of the redundancy to improve the yield [6], [7] or perform high-quality testing (either DFT or non-DFT) to increase fault coverage [8]. Testing core-based systems is a complex problem in general. It requires solving a multitude of tasks, such as test set generation and test response analysis, test scheduling, test access mechanism (TAM) design, and testability analysis [9]-[12]. Many of these tasks are facilitated by use of built-in self-test (BIST) that has become increasingly viable solution for testing complex SoCs. Although it is a promising technology it also has its problems, such as **very long test sequences**, and **random pattern resistant faults**. Therefore different approaches have been proposed, where pseudorandom test patterns are complemented with deterministic test patterns, which are applied from the ATE or, in special situations, from the on-chip memory. These approaches are generally referred to as **hybrid BIST** [13]-[17].

Novelty of the proposed research: The contribution of the project will be twofold. First, we propose to develop new methods and algorithms for testing complex NoC based SoCs. Second, we propose to develop novel NoC architectures that can efficiently be used for test data transportation (as TAM) and support different schemes for fault tolerance (either at the interconnect or core level).

Close cooperation in between TUT (Prof. R. Ubar) and Linköping University, Sweden (Prof. Z. Peng, Dr. G. Jervan) has given several original results in the area of hybrid BIST [13], [14], [18]-[23]. The results have been reported in many high-quality conferences, like DFT, ATS, ETS (acceptance rate

around 20-25%). The main results have been so far a set of novel test cost minimization algorithms under different design constraints (such as tester memory). These results have led to many **new challenges and opportunities**. For example, it is important to develop a test cost optimization framework, where more than one design constraint can be taken into account. This requires optimization over multiple domains, such as test quality, test length, testing time, memory cost, power constraints, area overhead, etc. These requirements are defined by the overall requirements of the resulting system, such as price, mobility (low energy consumption), speed, fault tolerance, etc. The research in this multidimensional space is new and a general theory is yet to be developed. The whole problem is very complex. It should be attacked step by step. Several new problems are already under investigation and the first results will be submitted to the upcoming conferences in very near future.

The novelty of our proposal related to the **network-on-chip** based on-chip communication infrastructure is the reuse of the on-chip network also for test data transportation. Modern SoCs are based on a single broadcast medium, such as AMBA and silicon backplane buses, with additional wiring for TAM implementation. Such schemes can no longer deliver the required global bandwidth and latency for current SoCs. The main goal of our approach is to improve already proposed on-chip interconnect architectures (NoCs) or to develop entirely new ones in order to facilitate test data transportation over the same communication lines, without need for extra wiring. Therefore, architectural design and test design tasks should be considered as a whole. It requires solving different tasks, such as design of an appropriate infrastructure (NoC that can function as a functional communication medium, as well as a TAM), its optimization and appropriate test set generation. The work will be performed with special emphasis towards hybrid BIST.

Built-in self repair (BISR) of permanent faults is "state-of-the-art" for memories. BISR of logic circuits is a known practice for FPGA-based designs, but not for ordinary cell-based logic designs. In their essence NoC-based designs share many similarities with FPGA-based designs and therefore also the BISR possibilities for NoC-based designs should be investigated. Most importantly, multi-core systems may also contain redundant hardware, making thus on-line repair possible. The important tasks here are the fault detection and on-line replacement strategies. So far, a circuit and system architecture that can ensure a dependable system operation based on not highly dependable hardware is not in reach.

The project requires implementation of several software and hardware modules (using FPGA-s) and a lot of experimental work. Therefore it is planned to involve to the project several bachelor and master students. Their involvement would give to the students a possibility for closer cooperation with faculty and the resulting implementations could be reused in different courses as well as in final theses. This strategy of combining research with teaching, and implementing the research results into the teaching environment will be also in the focus of the project.

Preliminary results achieved already: We have several preliminary results in this field. The research in the field of hybrid BIST has been carried out in cooperation with TUT while the grant applicant was associated with Linköping University (LIU) [13], [14], [18]-[23]. We have developed a very good laboratory research environment with a large set of diagnostic software tools, that has made the cooperation between TUT and LIU very successful.

Due to the lack of graduate students the project will start small with only one graduate student T. Shchenova (maiden name Vassiljeva), who has already proven her excellence by valuable international publications [23], [24]. The research in hybrid BIST will also be one of the main topics of her thesis. It is planned to include several bachelor and master students during different phases of the project and most promising ones will be offered a possibility to join the project as graduate students.

The research has also generated interest from the industry. The department has long and strong links with Estonian company Artec Group and the results of the project are directly applicable to their products. In addition, there are contacts with Estonian National Development Centre ELIKO, Philips Research and Ericsson, who have all shown their interest towards the proposed topics.

All the mentioned results achieved by now, and the high interest which has been expressed from the microelectronics industry create together an excellent motivation to continue this research towards developing more efficient and exact methods for fault tolerant self-testable digital systems.

c) Main goals, objectives and hypotheses of the project

The main goal of the current project is to develop new methods, algorithms and software tools for designing fault tolerant self-testable digital systems.
The main problems and objectives to be investigated are:

- development, evaluation and optimization of hybrid BIST methods for developing self-testable digital systems;
- development, evaluation and optimization of NoC architectures, where on-chip network can efficiently be reused for test data transportation;
- adaptation of developed hybrid BIST methods for proposed NoC architectures;
- development of new methods for fault tolerance in NoC based systems.

Hybrid BIST consists of pseudorandom and deterministic testing. Today's complex digital systems consist of multiple cores, where different approaches are possible: each core can have its own test resources, or the test resources are shared. Testing of cores can be carried out in parallel, in sequence, or in a combined parallel-sequential way. Pseudorandom and deterministic testing can be managed in a uniform way (either with shared resources, in parallel, or in sequence) or in a different way. The chosen strategy will affect differently to test length and time, power and energy consumption or memory cost and hardware overhead. A lot of different optimization tasks can be formulated, but all of them are very complex and don't have easy straightforward solutions. There are some solutions found in the literature for combinational cores. For sequential cores no systematic research has been made till now. The development of the complex optimization methodology, where several objectives can be considered simultaneously, will be one of the objectives of this project.

For estimating the solutions powerful test generation and fault simulation methods and tools should be available. Existing commercial tools work in connection with their generic design flow and are therefore not well suited for iterative optimization procedures (lack flexibility). The test generation and fault simulation tool environment that has been developed in the department [25] is better suited for the iterative use in the optimization procedures. This fact has been proved already in the cooperative research with Linköping University and Fraunhofer Institute in Germany. The high speed (comparable to the best commercial tools), efficiency and easy usability of our tools in complex iterative experiments has made the department attractive for foreign partners and offers very good opportunities for carrying out this project. Adding some new features to the diagnostic toolset will provide nice additional side-effect of the project.

NoC architectures and especially the possibility of reusing these for test purposes has been rather little investigated field. In this approach, instead of introducing new dedicated TAM to the system, the functional communication infrastructure of the system itself will be reused for testing purposes. This requires developing theoretical framework as well as a practical one. For the latter we see possibilities in FPGA-s and our aim is to develop an FPGA-based experimental environment for evaluation of different architectures.

This environment will also be used in research of different fault tolerance techniques. In this area the main objective is to investigate different self-repair mechanisms, based on redundancy (in case of faulty core) or rerouting (in case of error in wiring). As this domain is also relatively little investigated then most of the results have to be proven experimentally. Therefore the proposed FPGA-based analysis and synthesis environment is required.
To summarize, the project requires solving the following tasks:

- to investigate different cost factors of hybrid BIST solutions, such as hardware overhead, memory cost, testing time, fault coverage, power consumption, and others, with the goal to create proper models for test cost optimization;
- to develop methods, algorithms and tools for hybrid BIST optimization (with or without design constraints);
- to develop novel NoC architectures and corresponding synthesis and analysis methods for systems, where the same on-chip network is used for functional-mode communication, as well as for test data transportation;

- to adapt the developed NoC architectures for hybrid BIST ideology;
- to develop methods, algorithms and tools for optimization of the resulting solution (NoC architecture with corresponding hybrid BIST solution), such that different design constraints (such as energy or memory consumption, are overhead or others, are satisfied)
- to develop new test generation, fault simulation, test ordering, cost calculation, and design synthesis and analysis tools together with experimental research environment suitable for carrying out the synthesis and optimization procedures;
- to develop fault/error management systems that combine test, redundancy administration and controls repair extensions, also re-scheduling of tasks under error conditions.
- to develop methods, algorithms and tools for diagnostic test and self-repair for logic blocks and interconnects.

As an outcome of the work described, we will have a set of new concepts, methods, algorithms, and tools for supporting design of fault tolerant self-testable digital systems.

d) Research methods and equipment resources

Research methods are based on using digital electronics, automata theory, Boolean differential algebra, graph theory, theory of algorithms, combinatorial optimization theory, data structures and computation theory and other related fields of electrical engineering, computer science, software engineering and technical diagnostics.

Experimental investigations of new algorithms and procedures will be carried out by using the in-house software from TUT and LIU, as well as with professional CAD software from companies Cadence, Synopsys, Mentor Graphics, Xilinx and others that is available at the department and acquired via the EUROPRACTICE initiative. For experimental investigations, internationally recommended and accepted benchmark examples, such as ISCAS, ITC and others will be used. In addition, we foresee a possibility to use also industrial design examples from our industrial partners. In the framework of research and development infrastructure development programme we intend to build up also an environment for rapid prototyping (FPGA-based). This environment will be used for analysis and synthesis of different hardware platforms and has therefore crucial role for the project.

e) Institutions and researchers involved in the project

Initially, the following researchers and students of the TUT's Computer Engineering Department will participate in the project:

1. Gert Jervan	Ph. D.	Extraordinary senior research fellow
2. Peeter Ellervee	Ph. D.	Professor
3. Tatjana Shchenova	M. Sc.	Ph. D. Student (2005-2009)

The grant applicant Dr. Gert Jervan is a co-supervisor of the mentioned graduate student T. Shchenova, whose research topic is related to hybrid BIST methods and algorithms. Her Ph. D. studies are continuation of her master thesis that was investigating one of the sub-problems of hybrid BIST – energy minimization. Her master thesis was written in close cooperation with researchers from Linköping University (Prof. Z. Peng and Dr. G. Jervan) and many experiments were performed during her stay at Linköping.

Prof. Peeter Ellervee has long track record in synthesis and analysis of digital systems (and SoCs). His background is vital for carrying out work in the domain of NoC architectures, hardware synthesis and prototyping. The latter is also supported by his project entitled "FPGA Based Environment for Design Validation" (submitted to the ETF).

In order to achieve the results, it is needed to develop different software tools and to synthesize various hardware modules. For these implementation tasks several bachelor and master students will be included during different phases of the project and most promising ones will be offered a possibility to join the project as graduate students.

The current plan requires inclusion of at least one new graduate student during the second year of the project (to work mainly with NoC architectures) and another one should be included during the third year to work mainly with fault tolerance issues.

The activities of the project will be carried out in a close cooperation with Linköping University in Sweden. Dr. Gert Jervan has very long and strong connections with the named university (was working there last 7 years), that has been documented in more than 20 conference papers and 2 book chapters. Several TUT students have stayed in Linköping while writing their bachelor or master theses and also T. Shchenova's master thesis was largely written during her stay in Linköping.

In addition we foresee closer cooperation with Politecnico di Torino (ITA), Southampton University (UK) and Cottbus University (GER), and companies such as Artec Group (EST), ELIKO (EST), Philips Research (NED), and Ericsson (SWE).

f) Prognosis of publishing and implementing of project results

It is expected to publish annually at least 3-4 papers on current research results in internationally recognized journals and peer-reviewed conference proceedings. It is also expected to introduce the developed experimental diagnostic software and rapid prototyping environment into the teaching process at TUT (and other European universities, if possible).

The results could also be used by the Estonian and international companies. Our department has tight cooperation (in the framework of different projects) with Estonian companies Artec Design and ELIKO. The expected results of the proposed project can be used for developing novel fault tolerant self-testable digital systems and for improving the tolerance and efficiency of testing of their existing products.

g) Importance of the research for science and Estonian economy

The general importance of this research for scientific and industrial community of microelectronics lays in the development of a new concepts, methods, algorithms and software for design of fault tolerant self-testable digital systems. As it was mentioned earlier, we have close cooperation with different Estonian companies that can use the expected results of the proposed project for improving their competitiveness in the world market.

Secondly, the project has also educational aspects. The developed tools can be used for improving the quality of different test related courses in TUT and other universities. The obtained results can improve also the competence level of the group and to make it more attractive for different European project teams. This would help to find additional funding from different EU sources. As a general result of this type of knowledge and technology transfer, the teaching environment at the Computer Engineering Department will be continuously updated and held at the international level, which means great importance for educating students with professional skills on the international level. This fact will also have great importance for Estonia in the long-term sense – in appearing of new competitive SMEs in the Estonian electronics industry.

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2. Time Schedule of the Project

Year/Activity	Theoretical	Practical	Experimental
2006	– Research of different hybrid BIST cost factors – Modeling of different hybrid BIST parameters	– Software for hybrid BIST optimization	– Experiments with different hybrid BIST architectures for SoCs. – The results will be documented in three scientific papers (at least)
2007	– Analysis and modeling of novel NoC architectures – Adaptation of developed NoC architectures for hybrid BIST	– Development of the rapid prototyping environment – Software for hybrid BIST in NoC environment	– First experiments with rapid prototyping environment – Evaluation of hybrid BIST for NoC – The results will be documented in 3-4 scientific papers (at least)
2008	– Hybrid BIST optimization for NoC – Research in different fault tolerance techniques	– Software for hybrid BIST optimization in NoC environment	– Experimental evaluation of different optimization methods – The results will be documented in 3-4 scientific papers (at least)
2009	– Fault tolerant NoC architectures	– Software for synthesis of fault tolerant NoCs	– Quality analysis of synthesized NoCs. Joint experiments with fault tolerant NoCs and hybrid BIST – The results will be documented in 3-4 scientific papers (at least)