Silicon Photonics Chiplets for Scaling AI and the Cloud – Technology, Design, and Test

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Abstract
Artificial intelligence and cloud computing are driving an exponentially growing demand for optical interconnect bandwidth. From the datacenter network down to the chip level, silicon photonics is a prime technology to scale optical interconnects to the desired bandwidth density (>1 Tbps/mm), power consumption (<1 pJ/bit), and cost (<0.1 $/bit). In this presentation, we give an overview of imec’s Silicon Photonics Platform (iSiPP), designed to realize optical I/O scaling by leveraging established CMOS manufacturing and advanced 3-D integration methods. We will discuss recently developed silicon photonics chiplet technology, featuring high-speed silicon optical devices, high-speed through-silicon vias (TSVs), and low-loss fiber coupling structures. We will describe existing electro-optical testing solutions and highlight some of the future testing needs.

Biography Speaker
Joris Van Campenhout is Fellow Silicon Photonics and Director of the Optical I/O industry-affiliation R&D program at imec, which covers the development of an industrially scalable short-reach optical interconnect technology based on silicon photonics. Prior to joining imec in 2010, he was a post-doctoral researcher at IBM’s TJ Watson Research Center (USA), where he developed silicon electro-optic switches for chip-level reconfigurable optical networks. He obtained a PhD degree in Electrical Engineering from Ghent University (Belgium) in 2007. Joris was granted nine patents and has (co-)authored over 100 papers in the field of silicon integrated photonics, which have received 9000+ citations.

See also:
- https://scholar.google.be/citations?user=h5GdrsYAAAAJ