Title
Probing Complexities of 3D-Stacked ICs – A Test Engineers’ Perspective

Authors
Ferenc Fodor, Bart De Wachter, Arnita Podpod, Michele Stucchi, Erik Jan Marinissen
imec, Kapeldreef 75, 3001 LEUVEN, Belgium

Abstract
Advancements in processing and scaling of through-silicon vias (TSVs), die- and wafer stacking, and general wafer processing techniques have opened the door towards ICs built by vertically stacking dies. Accompanied by standardized memory interfaces such as JEDEC’s Wide-IO and HBM, which consist of large arrays of fine-pitch micro-bumps, the semiconductor industry has created the building blocks for 3D-SICs. Benefits include heterogeneous integration of multiple dies with a reduced footprint and higher product yield with high-density, high-performance low-power interconnects.

Pre-bond test of these dies, i.e., testing prior to stacking, is vital to achieve an acceptable compound stack yield. To keep the associated costs acceptable, it is best to get pre-bond test access to the dies by probing directly on their large-array, high-density micro-bumps. As research institute with a mission to develop industry-relevant solutions, imec has challenged various suppliers in the wafer probe industry to address the challenges associated to probing on large arrays of fine-pitch micro-bumps. Several suppliers responded and imec has worked with them to co-develop and demonstrate high-accuracy wafer probe stations and advanced fine-pitch probe cards. This joint development work has contributed to the industrial uptake if 3D-SIC products, especially amongst the big hitters of the memory industry. Today, pre-bond die test through micro-bump probing is commonplace.

However, there are more challenges involved in testing complex 3D-SICs. Mid-bond tests of partially assembled stacks offer valuable information about the stacking process, while they also help to ensure a high product quality of the final stack products. Mid-bond tests come with their own set of probe challenges, e.g., in the form of thinned and flexible samples on tape frames.

In this presentation, we will use imec’s in-house wafer manufacturing and stack assembly flow of a seven-die flip-chip fan-out wafer-level package (FC-FOWLP) 3D-SIC with a complex stack architecture as a framework to illustrate typical 3D probing challenges that we encountered and how we were able to address them in collaboration with our suppliers.