With the slowing of Moore’s Law, the industry is adopting a variety of advanced packaging methods to further advance heterogeneous integration of both logics and memory device. The breakthrough of 2.5D and 3D wafer level packaging technologies has opened up many new possibilities and test challenges. The vertically stack ICs and proximity of fanout methods on a small form factor package drive the need for a faster test speed with higher signal performance. A new level of advance probe card technology is required to address the required signal quality and the ability to successfully probe on TSV micro-bump structure in an ultra-low pitch grid array. This paper discusses test solutions for High-Bandwidth-Memory in various configurations and the implications on cost of test.