IEEE Std 1838 Introduction and the Move from a 1500-Centric TAM

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The IEEE standard for test integration of stacked ICs has been released and is rapidly being leveraged for test access in 3D stacked die and even 2.5D package applications. IEEE Std 1838™-2019, “IEEE Standard for Test Access Architecture for Three-Dimensional Stacked Integrated Circuits”, enables EDA tools to be automated to insert the standard so that designers can focus on functional innovation while having confidence in the fact that test access is available to help prove product quality. IEEE 1838 provides a mandatory serial data path and an optional parallel data path for test pattern application. The serial data path is implemented as a branch of IEEE 1149.1 using optional concepts further fleshed out in IEEE 1687.

This presentation will also update you on the architecture of IEEE Std 1838, provide some interesting development history, and explore some automation to help implement it in your next multi-die package project. The standard was not always heading in the direction that it ended up. This presentation will provide a background and some historical context to bring it to the point at which the published standard is now. For example, the initial direction that IEEE 1838 was heading involved using IEEE 1500 as the serial path interface between dies. It now uses IEEE 1149.1 and the SIB (Segment Insertion Bit) concept from IEEE 1687 to form that bit of the serial infrastructure. It will also lightly delve into some electronic design automation tools that will help implement the architecture for each die, and validate the implementation at the stack level.