IEEE Std 1838 Introduction and the Move from a 1500-Centric TAM
Serial and Parallel Port Introduction and Discussion

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3DC-TEST 2020
Package Possibilities

- 2.5D, 3D, 5.5D: many topologies
- Digital + memory is most prevalent
- Heterogeneous technology nodes
- Higher bandwidth
- Smaller footprint
- Lower power

Test Context

Functional (DFT) logic

Scan → Compression
Logic BIST → Memory BIST
Interconnect Test
Interconnect Test
Logic BIST → Memory BIST
Scan → Compression
Access Issues and Solutions

- TSVs not accessible
- Contacts too small and close together
- Contacts disappear

Die-Level Pre-Bond Test
Partial Stack Mid-Bond Test
Complete Stack Post-Bond Test
Access Issues and Solutions

- Complete Stack Post-Bond Test
- Final Package Test
- System-Level Test

Board
Serial Port

*Mandatory*
Each Die Has a Primary TAP
Figure 2 from IEEE Std 1838
Serial Access Up and Down
Multi-Tower Support
Serial Access to Die Wrapper Register (DWR)
IEEE Std 1838 Serial Path – This Die
IEEE Std 1838 Serial Path – That Die

STDO  STMS  STCK  STRSTN  STDI  

3DCR  FPPCONFIG  DR  BYPASS  

PTAP  DECODE  IR  

TDI  TMS  TCK  TRSTN  TDO
Die Wrapper Register

1. STAP₁

2. STAP₂

3. PTAP₃

Primary

Secondary

C1

C2

C3

PTAP

WSP

TMS

TCK

TRSTN

TDO
Pre-DFT Functional Path
Typical Dedicated Wrapper Cell at Boundary
Ignoring the “Analog” Component
Typical Shared Wrapper Cell
Inland Wrapping

Shore-Level Components
Constrained Inland Wrapping
Delay Test with No Inland Wrapping
Delay Test Penalty
Flexible Parallel Port (FPP)

Optional
Parallel Access
Flexible Parallel Port Lane Concept

Lane

FPP_SEC

Secondary Port

FPP_FROM_SIDE → FPP_TO_SIDE

FPP_FROM_CORE → FPP_TO_CORE

FPP_CLK_IN → FPP_CLK_OUT

FPP_PRI → Primary Port

die
Design Specifications

- Flexible Parallel Port (FPP) control registration (driving signals labelled “Control”, below) can be distributed
Registered Lane, Up Only

Lane

FPP_SEC

FPP_SEC_EN

FPP_REGN_BYP

FPP_TO_CORE

FPP_CLK_IN

FPP_PRI

FPP_REGPU_BYP

die
Non-Registered Lane, Down Only
FPP Application

- Functional (DFT) logic
- Scan Chains
- Test Modes
FPP Broadcast Application

Functional (DFT) logic
1500 vs. 1149.1
## 1149.1-Based vs. 1500-Based Solutions

<table>
<thead>
<tr>
<th></th>
<th>1149.1</th>
<th>1500</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Pins Required</strong></td>
<td>5</td>
<td>5/bottom die, 8/other die</td>
</tr>
<tr>
<td><strong>Timing closure</strong></td>
<td>1 signals: TMS → TCK</td>
<td>4 signals: SelectWIR, CaptureWR, ShiftWR, UpdateWR → WRCK</td>
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<tr>
<td><strong>Area overhead</strong></td>
<td>TAP controller + 5 TSVs on each die</td>
<td>8 TSVs on each die</td>
</tr>
<tr>
<td><strong>Test pattern reuse</strong></td>
<td>Yes, reuse die level tests at stack and package level</td>
<td>More complicated pattern reuse for arbitrary state transitions</td>
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Stack Under Discussion

1149.1

**TAP4**

- Primary: TDI, TMS, TCK, TRST*, TDO
- Secondary: TDQ, TMS, TCK, TRST*, TDI

1500

**TAP3**

- Primary: TDI, TMS, TCK, TRST*, TDO
- Secondary: TDQ, TMS, TCK, TRST*, TDI

**TAP1**

- Primary: TDI, TMS, TCK, TRST*, TDO
- Secondary: TDQ, TMS, TCK, TRST*, TDI

1149.1

- WSI, SelectWIR, WRCK, WRSTN, CaptureWR, ShiftWR, UpdateWR, WSO

1500

- WSO, SelectWIR, WRCK, WRSTN, CaptureWR, ShiftWR, UpdateWR, WSI
TAP Access Per Die

TAP4

TAP3

TAP1

TDI  TMS  TCK  TRST*  TDO

WSO  SelectWR  WRCK  WRSTN  CaptureWR  ShiftWR  UpdateWR  WSI
TMS Load to TCK
1500 Access Per Die
1500 Signal Paths

1500 Wrapped Core

Optional User Defined Wrapper Parallel Port (WPP)

Functional Inputs
Wrapper Boundary Register
Wrapper Bypass Register
Wrapper Serial Input (WSI)

Core FI
Test Enable(s)

Test Inputs (TI)
Test Outputs (TO)

Functional Outputs
Wrapper Boundary Register
Wrapper Instruction Register
Wrapper Serial Output (WSO)

Wrapper Serial Control (WSC)
Mandatory Wrapper Serial Port (WSP)
1500 Wrapped Core

Optional User Defined Wrapper Parallel Port (WPP)

Functional Inputs
Wrapper Boundary Register
Wrapper Bypass Register
Wrapper Serial Input (WSI)

Test Inputs (TI)
Test Outputs (TO)
Core Inputs (FI)
Core Outputs (FO)
Test Enable(s)

Wrapper Serial Control (WSC)
Mandatory Wrapper Serial Port (WSP)

(Optional) Parallel Capture Data

 Wrapper Serial Output (WSO)

Wrapper Instruction Register

Boundary Register

Serial SHIF Port
WR/WRO
RSK
WRSTN

3D Chiplet Test
Stack with 1500
Stack Under Discussion

TDI TMS TCK TRST* TDO

TAP4
TAP3
TAP1
TAP on Every Die
Memory with 1500 on TOP

Example Interface

WSI SelectWIR WRCK WRSTN CaptureWR ShiftWR UpdateWR WSO

TAP3

TAP2

TAP1

TDI TMS TCK TRST* TDO

WSPI

WSPI

WSPI

WSPI
Quick Evolution

= 1500 bus
Die-Level Cores Accessed with 1500
Stacked and Electrically Connected
1149.1 Controller Drives WSP
## 1149.1-Based vs. 1500-Based Solutions

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Implementation
IEEE Std 1838 Serial Path – DFT Synthesis
Stack-Level Validation

Framework for any type of multi-die design
Thank You

Please address questions to a.cron@ieee.org