Designing Testable Systems With Chiplets

Active silicon interposer enables rapid development of SiPs and Chips using chiplets in a modular style but more importantly allow additional abilities for system testability. zGlue’s active silicon interposer, Smart Fabric, is used as a base chip to enable chiplet stacking, system power delivery, connectivity, and other management functions needed for successful productization of chiplet-based systems. One such essential function is the distributed built-in self-test (BIST) function. Distributed BIST enables manufacturing yield enhancement and the use of loose tolerance manufacturing lines resulting in cost optimization. A key aspect of the zGlue interposer is its ability to work with off-the-shelf chiplets in known good die (KGD) and chip scale package (CSP) format without dictating a footprint constraint on chiplets. This is achieved by making a fine pitch bump array on the zGlue interposer. A single ball on the chiplet die comes in contact with multiple bumps on the zGlue interposer, later referred to as a ‘one-to-many’ scheme. This way a spatial over-sampling of the die solder-balls ensures that zGlue interposer can attach to off-the-shelf IO solder ball geometries. A localized switch underneath each zGlue micro bump can then be programmed to connect it to power, ground, and different signal buses. Connection to the RF and sensitive analog signals are handled in RDL. The programmability of Smart Fabric bumps also opens up the possibility of repair after manufacturing. A scheme for electronic realignment makes it possible to compensate for the X, Y, and angular misalignment in the attachment of dies to a certain degree which alleviates one of the key manufacturing challenges. An important feature of the technology is the footprint agnostic assembly of components in a cost-conscious and high-volume compatible manner.

Another key aspect of this built-in self-test scheme augments the system level-test of the final assembly. BIST is implemented as a distributed feature to test open circuit, short circuit, and ohmic values before the system assembly or after the assembly and can take vectors piped in via a probe card or via package pins. Kelvin-probe formation underneath the chiplet IOs can help with failure analyses. Additionally, chiplet IOs can be probed selectively without the need for complicated test hardware. We have used such test mechanisms successfully for debug, bring-up, contact probe testing, as well as system-level structural testing. Additional functional features of Smart Fabric also help in testing of power scenarios, inter-chiplet connectivity, and functionality. With the successful delivery of the zGlue technology, a path to the development of a new area of 3D-IC has opened up. With this modular IC design style, we are able to support an ecosystem and effectively handle high-mix low volume devices that we expect with the growth of connected intelligent devices everywhere.

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