3DC-TEST

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Designing Testable Systems with Chiplets

Jawad Nasrullah, CEO, zGlue Inc

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Outline

• zGlue Integration Platform
• Active Interposer BIST
• Yield and Testing Considerations
• Reliability Testing and Procedures
zGlue—Custom Chips on Demand
zGlue integration Platform

Chiplet / Die

VDD1, VDD2, VDDn
GND
Analog Signal Fabric
Digital Signal Fabric

OTP  Control  Power Supplies  Peripherals

zGlue Smart Fabric
zGlue Smart Fabric Active Si Interposer

Programmable Routing Fabrics

a) Analog
b) Digital
Active Interposer Chiplet BIST Scheme

Built in Testability Functions with a matrix of Cu pillars

1. Open/Short
2. IDDQ
3. Connectivity
4. Programmable Probe
5. Kelvin
6. Pull up/pull down
7. Cap insert
8. Level Shift
9. Programmable IO
10. Chiplet VID

Support for 400um balls to <55um u-bump pitch
zGlue OmniChip Reference Design

SIP for Wearables, Fitness, Bio
CortexM4 MCU + BLE
Temperature Sensing
Vibration, Steps (Accelerometer)
Roll and Pitch (Compass)
Battery Recharging
Heart Rate Sensor
zGlue Chiplet BIST Scheme

CP: JTAG
SLT: JTAG, SPI, I2C
CP: Probe Points
SLT: Wirebond/TSV
zGlue Chiplet BIST and Repair Scheme
Debug Signal Fabric

Observe any signal within the smart fabric at the output using software reconfiguration.
Designing and Manufacturing Steps—Chips / Chiplets

**DESIGN STEPS**

1. Architecture, IP block selection, Package Selection, Technology Selection

2. Design Entry
   - IO Planning
   - RTL Design and Verification
   - Schematic Capture
   - Component Placement

3. Chip Layout / Routing / Package Layout

4. Verification
   - Functional
   - Electrical
   - Thermal

5. Send to Manufacturing

**MANUFACTURING STEPS**

1. Wafer Fab, Contact Probe (KGD?)

2. Package Fabrication (Optional), e-test

3. uBump/Assembly/CSP/BGA

4. Packaged Part Test

5. ESD and Latchup Tests (sampling)

6. Reliability Tests, HTOL (sampling)

7. Infant Mortality Burn-in

8. Final Test
Designing and Manufacturing Steps—Chiplet Integration

**DESIGN STEPS**

1- Architecture, Chiplet selection, Package Technology Selection

2- Design Entry
   - IO Planning
   - RTL Design and ESL Verification
   - Schematic Capture/Netlist Gen
   - Component Placement

3- Substrate/Interposer Routing and Layout

4- Verification
   - Functional
   - Electrical
   - Thermal

5- Send to Manufacturing

**MANUFACTURING STEPS**

1- Interposer Fab, Contact Probe

2- Substrate Fab, e-test

3- Chiplet Assembly/Packaging

4- Package Test

5- ESD and Latchup Tests (sampling)

6- Reliability Tests, HTOL (sampling)

7- Infant Mortality Burn-in
DFT & Verification:
- Need ESL (transaction level) and IBIS Models for all Chiplets
- Need Mechanical Models for all Chiplets for Thermal/Mech Simulations
- Simple JTAG in each Chiplet

Incoming Material:
- Visual Inspection
- Quality of Chiplets to be guaranteed by the Vendor
- E-test for substrate
- CP test for Si Interposer

After Assembly:
- Inspection (e.g. x-rays)
- System level testing to verify assembly process (JTAG needed)
- Reliability testing
Chiplet Integration Ops Flow

- Chiplet 1: CP, Package Test, Reliability, Final Test
- Chiplet 2: CP, Package Test, Reliability, Final Test
- Chiplet n: CP, Package Test, Reliability, Final Test
- Interposer Waf: CP Test
- Substrate: DPM_S (Inspection)

Component Suppliers: $$$
Chiplet Integrator: $$$

Assembly: DPM_C1 (Inspection), DPM_C2 (Inspection), DPM_Cn (Inspection)

SLT: Fallout FA, Reliability Testing

2L Interconnect Customer: $$$
Yield Estimation Example

Incoming DPMin Chiplet C1-C4= DPM_C < 100
Number of Chiplets = N = 4
Incoming DPM in Si Interposer = DRM_W <100

Failed Assemblies due to incoming DPM
= N x DPM_C+ DRM_W
= 4 x 100 + 100 = 500 (99.95%)

Control of Incoming DPM_C is the key for Yield.

Assembly Yield numbers can be awesome.

System Level Test is the key to control outgoing DPM
For Heterogeneous Chips.
Summary

• zGlue = Glue Chiplets in z Direction and Make Custom Chips with High Reliability.

• zGlue BIST is a key enabling technology for Chiplet Integration and production.

• Observability and Debug of Failures should be carefully planned. Built in Self Test schemes in active Silicon interposers are key enablers.

• IC Package Environmental Tests are critical to work out Chiplet Integration reliability concerns.

• System Level Tests can be the final shipping criterion.

• Beware of over-testing.

• Testing Technology available for licensing

For more info contact jawad@zglue.com
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Thank You