Universal Chip Telemetry™ (UCT) for Quality and Reliability Monitoring of 2.5D Packaging in 5nm and 7nm

Nir Sever, Sr. Director of Product
November 6, 2020
Risks in D2D Connectivity

Challenges in CoWoS
- Single u-bump per signal
- Quality issues can be related to:
  - u-bump cracks
  - Assembly defects

QnR challenges
- Lack of redundancy
- High density
- High speed
- Lack of visibility for latent defects

Challenges in InFO
- Single trace per signal
- Quality issues can be related to:
  - Open & short
  - Bridge-short (signal to signal or to supply)

Risk of expensive
- Quality escapes
- In-field degradation

Interconnect quality issues may lead to full system failure
Universal Chip Telemetry™ (UCT) for Visibility

- High resolution and widespread UCT Agents at no cost to area
- Mimic the design and monitor key parameters
- Operate in-situ and in mission-mode
- Readouts extracted using industry standard methods and formats
Proteus™ for Actionable Insights

UCT based Margin measurements

Insights
- Performance measurement per pin
- Eye diagram per pin
- Rx signal integrity
- Lane integrity (organic substrate)
- u-bump integrity (silicon interposer)
Proteus™ for D2D Connectivity

• General Purpose
  – InFO™, CoWoS™, 3DFabric™, Glink™, HBM3 and counting…
• Based on ongoing tracking of the signal timing at the receiver (margin to failure)
  – Per lane, in mission mode, and no impact on signal
• Wide speed range: 2GHz (4Gb/s DDR) to 8GHz (16Gb/s DDR)
• Full eye visibility for DDR signals:
  – Setup and Hold to positive and negative edges of reference clock
  – Keep track of min, max and average (“Jitter”)
• Same Agent, all signal types:
  – Rx only, Tx only and Bidirectional
  – Single-ended and Differential
  – Single side monitoring (e.g. HBM3) or both
Complete System Level Solution

- **IO Sensor:**
  - Area efficient, operates on VDD core; per process node Hard IP
  - Designed for integration inside PHY hard macro
  - One IO Sensor per pin

- **Agent controllers:**
  - Synthesizable RTL for simple IC integration
  - APB standard bus interface to Host CPU
  - JTAG and I2C interfaces for external control
Near End and Far End Monitoring

Operates in Mission Mode (no special test mode required)

Δ = NE Pulse Delay

Δ = FE rising edge delay
Providing Visibility of Lane Integrity

- Signal integrity grading
- Performance grading
Silicon Proven: Lane Grading

Per pin signal quality map*:

Measured in GUC’s 5nm HBM2E 3.2 Gbps Test Chip

* CoWoS lines were intentionally routed beyond their spec limits
High Coverage NPI

BKM

- Go / No Go
- Worst case margin per group
- Low coverage, low volume
- Time consuming
- Labor intensive

Low visibility → Low confidence

proteanTecs

- Parametric
- Full eye visibility per pin
- All pin coverage
- Fast, immediate, during standard test
- Analytics at the click of a button

High visibility → High confidence
Silicon Proven: Outlier Detection*

- Lane degradation monitoring and repair at test
- Based on Rx slew rate

Far-End Integrity Insight per Channel and Pins in Channel

Rx Signal Amplitude at Pin

Measured in GUC’s 7nm and 5nm HBM2E 3.2 Gbps Test Chips

* CoWoS lines were intentionally routed beyond their spec limits
In-field Degradation Monitoring & Predictive Maintenance

- Predictive maintenance
- Alerts on faults before failures
- In mission mode

Lane Integrity

- Integrity insight
- Degradation threshold

Proteus Alert

System failure

Time
Silicon Proven: Degradation Monitoring

- Lane degradation monitoring and repair, in mission-mode*
- Based on near-end and far-end integrity insights

Measured in GUC’s 7nm and 5nm HBM2E 3.2 Gbps Test Chips

* ASIC buffer strength intentionally weakened to emulate u-bump resistance change
Thank you.