Session 7: Panel

Test Challenges in the New 3D and Chiplet World

Moderator: Jan Vardaman – President – TechSearch International (USA)

Panelists:  
- Dave Armstrong – Director of Business Development – Advantest (US)  
- Paul Franzon – Professor, Director of Graduate Programs – NCSU (US)  
- Bob Patti – President – NHanced Semiconductors (US)  
- John Yi – PMTS Product/Test Engineering – AMD (US)
Test Challenges in the New 3D and Chiplet World

E. Jan Vardaman
Moderator

- TRACK INNOVATION
- IDENTIFY TRENDS
- ANALYZE GROWTH
- INFLUENCE DECISIONS

RELEVANT, ACCURATE, TIMELY
Panel Members

- Dave Armstrong, Advantest
- John Yi, AMD
- Gerard John, Amkor Technology
- Bob Patti, NHanced Semiconductors
- Paul Franzon, North Carolina State University
Panel Questions

• What is different between 3D-stacked ICs and chiplet-based ICs?
  – Are there differences in technology, design, manufacturing flow, and especially test: Test flows, DfT, probing etc.?
  – What test/DfT technology do we need for chiplet-based ICs that we did not need for “conventional” 3D-ICs?

• What new test equipment is required for this new era of chiplets and 3D (or is what we have adequate)?

• Do we need Known Good Die or Chiplets or is Probably Good Die Sufficient? What level of testing is sufficient? Test interfaces? System test?

• Several companies indicate they are using AI-solutions to help with their test strategy, what solutions are you aware of?

• Are new probe methods needed?

• What is the role of inspection and what kind of inspection technology is required?