Seventh IEEE International Workshop on Testing Three-Dimensional, Chiplet-Based, and Stacked ICs

virtual workshop, continuation of the popular 3D-TEST Workshop in conjunction with IEEE International Test Conference / Test Week 2020

November 5+6, 2020
http://3dtest.tttc-events.org

Call for Participation

The 3DC-TEST Workshop focuses exclusively on test of and design-for-test for three-dimensional, chiplet-based, and stacked ICs (3D-SICs), including systems-in-package (SiP), package-on-package (PoP), 3D-SICs based on through-silicon vias (TSVs), micro-bumps, and/or interposers. While these stacked ICs offer many attractive advantages with respect to heterogeneous integration, small form-factor, high bandwidth and performance, and low power dissipation, there are many open issues with respect to testing such products. The 3DC-TEST Workshop offers a forum to present and discuss these challenges and (emergent) solutions among researchers and practitioners alike.

3DC-TEST will take place in conjunction with the IEEE International Test Conference (ITC) and is sponsored by the IEEE Philadelphia Section in concurrence with the Test Technology Technical Council (TTTC).

Workshop Program – The workshop program contains the following elements.

- Keynote Address: Joris Van Campenhout, Fellow Silicon Photonics and Director Optical I/O Industry-Affiliation R&D Program at imec (Belgium): ‘Silicon Photonics Chiplets for Scaling AI and the Cloud – Technology, Design, and Test’;
- Six sessions encompassing 19 paper presentations;
- A panel discussion ‘Test Challenges in the New 3D and Chiplet World’ moderated by Jan Vardaman (TechSearch International) with panelists Dave Armstrong (Advantest), Paul Franzon (NCSU), Gerard John (Amkor Technologies), Bob Patti (NHaranced Semiconductors), and John Yi (AMD).

All presentations will be ‘live’. For the detailed version of the program, please see the next page.

Participation – You are invited to participate in the workshop. Participation requires registration and a registration fee. Workshop registration includes access to all technical sessions, Electronic Workshop Digest (containing extended abstracts, papers, slides, posters, as made available by their presenters). On-line registration is available via the workshop’s web site (http://3dtest.tttc-events.org).

Further Information

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Day 1: Thursday November 5, 2020

Session 1: Opening
Moderator: Saman Adham – TSMC (Canada)

17:00h: Welcome Address
General Co-Chair: Erikk Jan Marinissen – IMEC (Belgium)
General Co-Chair: Yervant Zorian – Synopsys (USA)

17:15h: Keynote Address: ‘Silicon Photonics Chiplets for Scaling AI and the Cloud – Technology, Design, and Test’
Joris Van Campenhout* – Fellow/Director – IMEC (Belgium)

Abstract: Artificial intelligence and cloud computing are driving an exponentially growing demand for optical interconnect bandwidth. From the datacenter network down to the chip level, Silicon Photonics is a prime technology to scale optical interconnects to the desired bandwidth density (>1Tbps/mm), power consumption (<1pJ/bit), and cost (<0.1$/bit). In this presentation, we will discuss recently developed silicon photonics chiplet technology, featuring high-speed silicon optical devices, high-speed-through-silicon vias (TSVs), and low-loss fiber coupling structures. We will describe existing electro-optical testing solutions and highlight some of the future testing needs.

18:00h: The SEMI Heterogeneous Integrated Roadmap
Test Working Group Update
Zoe Conroy* – Cisco Systems (USA)

18:15h: End of Day 1

Friday November 6, 2020

Session 2: Probing Chiplets and 3D Dies
Moderators: Gerard John – Amkor Technologies (USA);
Saghir Shaikh – Broadcom (USA)

10:00h: Probing Complexities of 3D-Stacked ICs – A Test Engineers’ Perspective
Fenere Fodor*, Bart De Wachter, Anita Podpod, Michele Stucchi, Erikk Jan Marinissen – IMEC (Belgium)

10:15h: HBM2 Probing Challenges and Probe Card Architecture
Raffaele Vallauro, Alessandro Antonioli, Flavio Maggioni – TechnoProbe (Italy)

10:30h: A New Age of IC Packaging – Test Complexity and Coverage on Advanced Packages and HBM
Quay Nhin – FormFactor (USA)

10:45h: Known Good Die (KGD) Strategies Compatible with Direct Hybrid Bonding
Emilie Bourjot*, Paul Stewart, Clément Castan, Loïc Sanchez, Gaelle Mauguen, Yorrick Exbrayat, Violal Balan, Nicolas Bresson, Amandine Jouve, Frank Fourmel, Florence Servant, Severine Cheramy – CEA-LETI (France); Nicolas Raynaud, Pascal Metzger – SET Corporation (France); Pascal Vivet – CEA-LETI (France)

Session 3: Chiplet DfT & BIST
Moderators: Adam Cron – Synopsys (USA);
Dheepak Jayaraman – Facebook (USA)

11:00h: Managing Test & Repair of Die-to-Die High-Speed Interfaces in the Chiplet Era
Mike Ricchetti*, Gurgen Harutyunyan, Yervant Zorian – Synopsys (USA)

11:15h: 3D Design-for-Test Solution for Chiplet-Based Active Interposer Architecture
Pascal Vivet – CEA-LETI (France), Jean Dunjot, Sebastien Thuret, Denis Dutot, E. Bourjot, S. Cheramy – CEA-LETI (France)

11:30h: BIST and BISR-Based 3DIC Interconnect Interface Test and Repair
Changming Gu*, Zhe Liu, Junlin Huang – HiSilicon Technologies (China)

11:45h: Process-Resiliant Fault and Error Tolerant DLL for Supporting Multi-Die Clock Synchronization
Jun-Yu Yang, Shi-Yu Huang* – National Tsing-Hua University (Taiwan)

Session 4: The New 3D-DfT Standard: IEEE Std 1838™
Moderators: Vivek Chickermane – Cadence Design Systems (USA);
Pascal Vivet – CEA-LETI (France)

12:00h: IEEE Std 1838™ Introduction and the Move from a 1500-Centric TAM
Adam Cron* – Synopsys (USA)

12:15h: Applying IEEE Std 1838™ to a 3DIC – A Case Study
Teresa McLaurin* – ARM (USA)

12:30h: Leveraging Lessons-Learned on 2D-SOCs in Designing Parallel TAMs Based on IEEE Std 1838’s Flexible Parallel Port for 3D-SICs
Erik Jan Marinissen* – IMEC (Belgium)

12:45h: Discussion

Lunch Break: 13:00-14:00h

Session 5: Intel Foveros
Moderator: Sreejit Chakravarty – Intel (USA); Teresa McLaurin – ARM (USA)

14:00h: Intel Foveros Technology: DfT And HVM Test Strategy
Wei Ming Lim*, Terrence Huat Hnin Tan, Sook Kwan Chese, Kian Lek Koy, Sreejit Chakravarty – Intel (USA)

14:15h: Who’s at Fault? A Creative Way to Isolate and Debug Internal IO Failures
Devanraj Sethuraman*; Ahmad Hiyamuddin Arshad – Intel (Malaysia)

14:30h: Pre-Silicon Validation Methodology Breakthrough for 3DIC
Yip Wei Loon*, Ng Hock Thien, Teo Biao Sim – Intel (Malaysia)

14:45h: Discussion

Session 6: 3D Chiplets Novel Approaches
Moderators: Marc Huter – Teradyne (Canada); Rajamani Sethuram – NVidia (USA)

15:00h: Bunch of Wire (BoW) Interchiplet Link Testing and Loopbacks
Shahab Ardalan*, Marc Huter, Bapi Vinnakota – Ayar Labs, Teradyne, Broadcom (USA, Canada)

15:15h: Designing Testable Systems With Chiplets
Jawad Nasrullah* – ZiGu (USA)

15:30h: Universal Chip Telemetry™ (UCT) for Quality and Reliability Monitoring of 2.5D Packaging in 5mm and 7mm
Nir Sevier* – ProteanTecs (Israel)

15:45h: System-Level Test for 3D-Multipich Modules
Sajjad Pagarkar* – Google (USA)

Session 7: Panel Session
16:00h: Test Challenges in the New 3D and Chiplet World
Abstract: As the industry moves to new architectures to achieve the economic gains previously achieved with scaling, a new era of chiplets, including 3DICs is emerging. Despite new names for packaging options, some issues remain — including test. The availability of known-good parts and a test strategy is still important. Co-design and design-for-test are essential. Developing a solution to allow the use of open market chiplets requires new strategies. This panel examines some of the issues related to test including alternatives to probing, developments in die sort, increased adoption of BIST, and the role of redundancy.
Moderator: Jan Vardaman – President – TechSearch International (USA)

16:15h: Closure of Workshop
General Co-Chair: Erikk Jan Marinissen – IMEC (Belgium)
General Co-Chair: Yervant Zorian – Synopsys (USA)

17:00h: End of 3DC-TEST Workshop 2020