

Mentor Graphics

 **TURBO TESTER**

Testing and DFT tools

(Installed in our PLD Lab)

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DFT Package tools

✓ DFT Advisor – insert internal scan circuitry

✓ BSD Architect – insert boundary scan circuitry

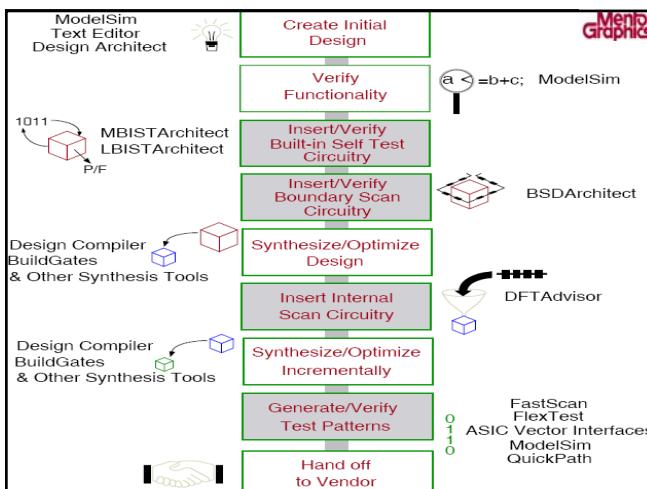
✓ Fast Scan – quick full-scan ATPG and fault simulator

✓ Flex Test – sequential ATPG and fault simulator

✓ LBIST Architect – insert logic BIST circuitry

✓ MBIST Architect – insert memory BIST circuitry

✓ Embedded Deterministic Test (EDT) and TestKompress
– generate and compress deterministic test patterns



The diagram illustrates the components of an ATPG library:

- Design** (represented by a blue cylinder)
- ATPG Library** (represented by a blue cylinder)
- Tools:** DFTAdvisor, FlexTest, LBISTArchitect, etc. (represented by a yellow cube)

Annotations provide additional context:

- Levels:** RTL, Gate (linked to Design)
- Formats:** EDIF, VHDL, Verilog, Genie, TDL, Model (linked to ATPG Library)
- A callout states: "ATPG library is NOT required if the design netlist fully defines all the primitives. (It can occur only in Verilog and TDL formats.)"
- Where to get one?**
- Three numbered steps for obtaining the ATPG library:
 - Use one preinstalled for Mentor Graphics training examples. To locate it use `find` command.
 - Use `class.atpglib` compatible with Turbo Tester class.lib (Synopsys) www.pld.itu.ee/~maksim/mg/class.atpglib
 - Create your own for your particular library:
 - Manually
 - Use `LibComp` to translate it from Verilog

```
> find /cad/m_04/ -name atpglib -print
/cad/m_04/dft/shared/pkgs/testkompress,ss5/systest_data/atpglib
```

MG DFT Documentation

✓ Local
[/cad/m_04/dft/shared/pdfdocs](file:///cad/m_04/dft/shared/pdfdocs)

✓ Mentor Graphics SUPPORTNET (requires free registration)
<http://www.mentor.com/supportnet/>

✓ External storage of Mentor Graphics Design-for-Test '99 documentation:
<http://www.fm.vslib.cz/~kes/bs/mg/mg.html>



```

graph TD
    DFTCompiler[DFT Compiler] --> RTLDRC[RTL TestDRC  
Full-Scan DFT  
AutoFix]
    RTLDRC --> Netlist[Netlist w/scan]
    RTLDRC --> STIL[STIL Protocol]
    RTLDRC --> Verilog[Verilog or SystemVerilog Library]
    Netlist --> TetraMAX[TetraMAX]
    STIL --> TetraMAX
    Verilog --> TetraMAX
    TetraMAX --> ATPG[High-Performance ATPG]
    TetraMAX --> GUI[Integrated GUI]
    TetraMAX --> FaultSim[Fault Simulator]
    ATPG --> TestVectors[Test Vectors]
    GUI --> TestReports[Test Reports]
    FaultSim --> TestReports
  
```

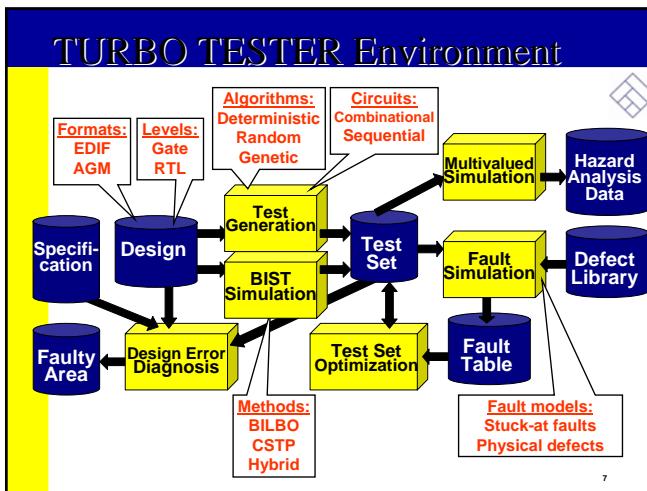
The diagram illustrates the architecture of the Synopsys TetraMAX ATPG tool. At the top is the "DFT Compiler" which contains "RTL TestDRC", "Full-Scan DFT", and "AutoFix". Arrows point from "RTL TestDRC" down to three separate components: "Netlist w/scan", "STIL Protocol", and "Verilog or SystemVerilog Library". These three components all have arrows pointing to the central "TetraMAX" block. The "TetraMAX" block is shown in a light blue box and contains three stacked sections: "High-Performance ATPG", "Integrated GUI", and "Fault Simulator". From the bottom of the "TetraMAX" block, three arrows point down to three separate boxes at the bottom: "Test Vectors", "Test Reports", and another "Test Reports" box. The "Integrated GUI" section also has an arrow pointing to its own "Test Reports" box.

Synopsys TetraMAX

Offers a choice of ATPG modes:

- Basic-Scan ATPG**, an efficient combinational-only mode for full-scan designs
- Fast-Sequential ATPG** for limited support of partial-scan designs
- Full-Sequential ATPG** for maximum test coverage in partial-scan designs

It is integrated with **Synopsys' DFT Compiler**.



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