Testing and DFT tools

(Installed in our PLD Lab)

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DFT Package tools

- ✓DFT*Advisor* – *insert internal scan circuitry*
- ✓BSD*Architect* – *insert boundary scan circuitry*
- ✓Fast*Scan* – *quick full-scan ATPG and fault simulator*
- ✓Flex*Test* – *sequential ATPG and fault simulator*
- ✓LBIST*Architect* – *insert logic BIST circuitry*
- ✓MBIST*Architect* – *insert memory BIST circuitry*
- ✓Embedded Deterministic Test (EDT) and Test*Kompress*
  - *generate and compress deterministic test patterns*

```
server:/home/user>cat .cshrc
…
setenv MENTOR
setenv MENTOR_64
…
```

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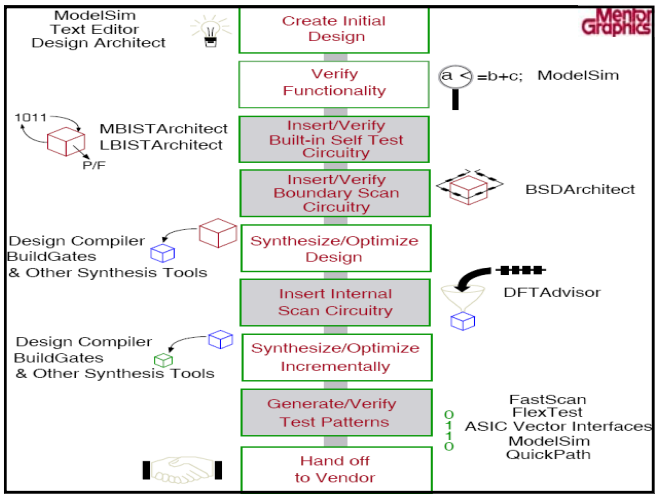
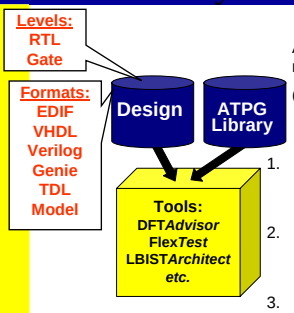


ATPG library



ATPG library is **NOT** required if the design netlist fully defines all the primitives.

(It can occur only in Verilog and TDL formats.)

Where to get one?

1. Use one preinstalled for Mentor Graphics training examples.
   To locate it use ***find*** command.
2. Use **class.atpglib** compatible with Turbo Tester class.lib (Synopsys)
   www.pld.ttu.ee/~maksim/mg/class.atpglib
3. Create your own for your particular library:
   a. Manually
   b. Use *LibComp* to translate it from Verilog

```
> find /cad/m_04/ -name atpglib -print
;...
/cad/m_04/dft/shared/pkgs/testkompress.ss5/systest_data/atpglib
```

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MG DFT Documentation

- ✓**Local**
  `/cad/m_04/dft/shared/pdfdocs`
- ✓**Mentor Graphics SUPPORTNET (requires free registration)**
  http://www.mentor.com/supportnet/
- ✓**External storage of Mentor Graphics Design-for-Test '99 documentation:**
  http://www.fm.vslib.cz/~kes/bs/mg/mg.html

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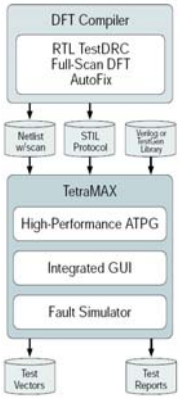
Synopsys TetraMAX



Offers a choice of ATPG modes:

- **Basic-Scan ATPG**, an efficient combinational-only mode for full-scan designs
- **Fast-Sequential ATPG** for limited support of partial-scan designs
- **Full-Sequential ATPG** for maximum test coverage in partial-scan designs

It is integrated with ***Synopsys' DFT Compiler.***

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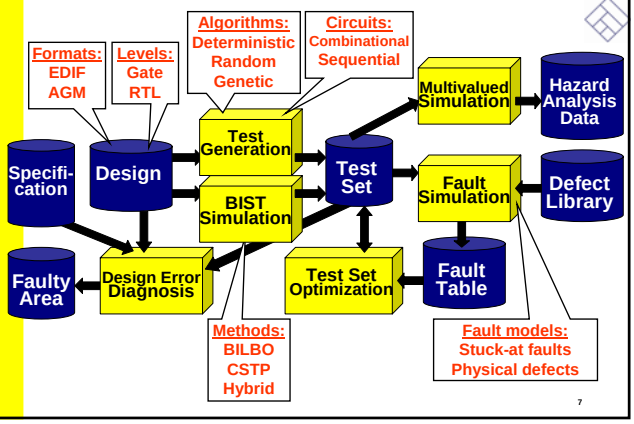
TURBO TESTER Environment



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