Texas Instruments

MSP430FE42x(A) ESP430CE1(A) Peripheral Module

User's Guide

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Chapter 1

ESP430CE1(A)

The ESP430CE1(A) module incorporates the SD16, hardware multiplier, and ESP430 embedded processor engine for use in single-phase energy metering applications. This chapter describes the ESP430CE1 and its enhancement to the ESP430CE1A. The ESP430CE1 and the ESP430CE1A modules are implemented in the MSP430FE42x and MSP430FE42xA devices, respectively.

Topic **Page**

1.1 ESP430CE1(A) Introduction

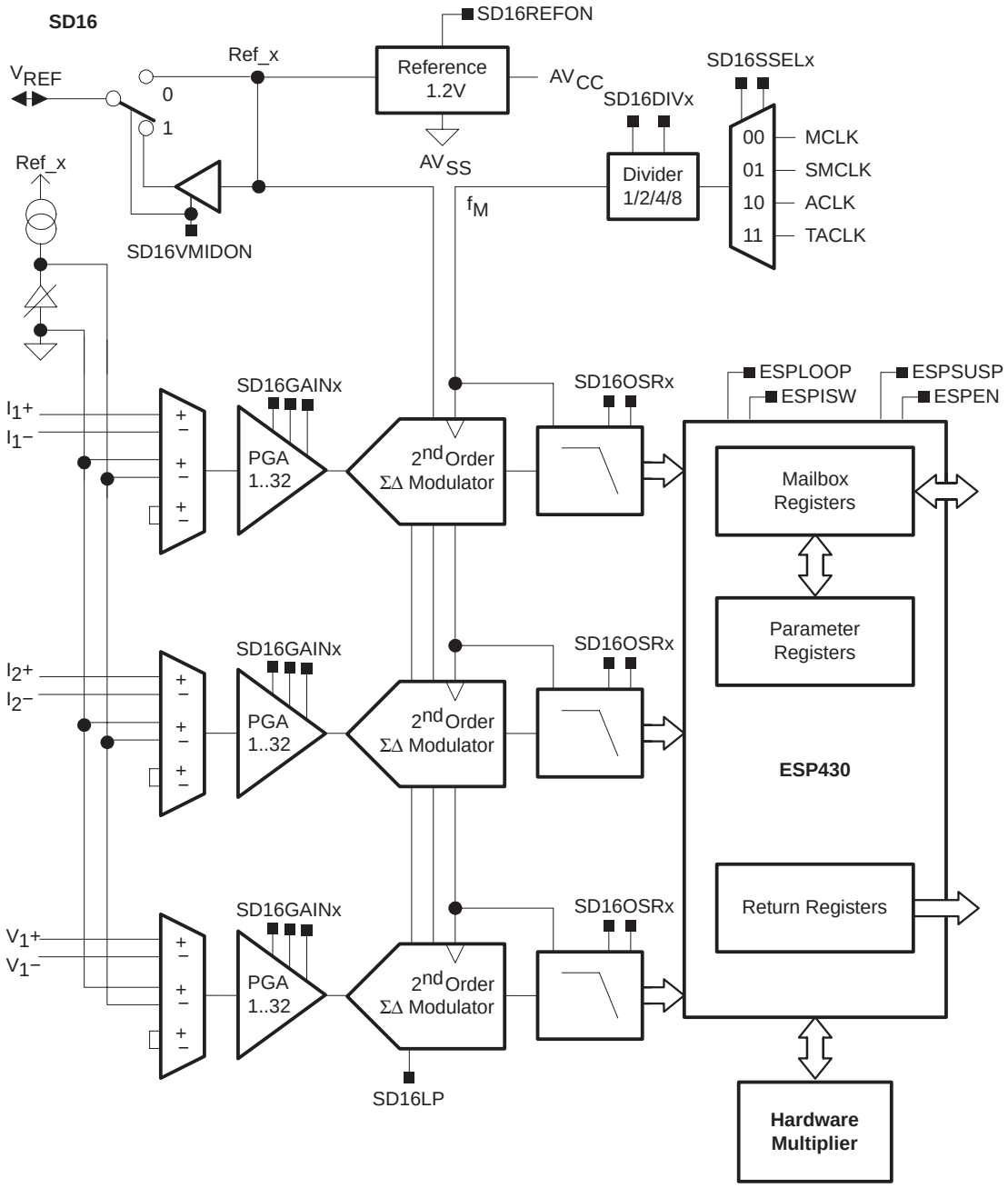
The ESP430CE1(A) module is designed to perform energy metering calculations independently of the CPU. The module includes the SD16 module, Hardware Multiplier module and the ESP430 embedded signal processor.

Features of the ESP430CE1(A) include:

- Complete analog and digital functionality for single-phase metering (2-wire and 3-wire applications)
- Tamper detection functionality
- Built-in calibration features and flexible user-configurable system setup
- Integrated analog front end (AFE) for voltage and current sampling
- Independently configurable analog input gain and oversampling ratio
- Software selectable internal or external voltage reference
- Built-in temperature sensor
- Integrated processing for metering calculations including active, apparent and reactive energies, power factor, line frequency, etc.
- Direct interface to hardware multiplier module

The block diagram of the ESP430CE1(A) module is shown in Figure 1−1.

Figure 1−1. ESP430CE1(A) Block Diagram



The following are the key differences/improvements to the ESP430CE1A in comparison to the ESP430CE1:

- The digital integrator to support Rogowski coils is not implemented.

  Rogowski coils can be connected using an external analog integrator.

- Spikes on voltage V_1 can disturb the measurement of the mains period leading to incorrect results that use this information. A programmable V_1 filter can be used to eliminate such spikes. See section 1.2.11 “Maximum Spike for V_1 Filter” for details

- The reactive energy algorithm is improved and the result is signed. See section “Reactive Energy” for details.

- The apparent energy algorithm is improved and calculated using reactive and active energy.

- The three ADC offsets N_{V1SC}, N_{I1SC}, and N_{I2SC} to measure V_1, I_1, and I2, respectively, are initialized with zero instead of measuring them with the ADC inputs shorted. See section “Control Register 0” for details.

- The ADC values for the I_1 and I_2 samples are saturated to 7FFFh (maximum positive value) and 8000h (max. negative value) during sample preparation (saturation).

- A watchdog function observes the zero crossing of V_1. If zero crossings are missing (e.g., due to a defective resistor divider) the watchdog expires and triggers the DC removal calculations associated with a zero crossing.

- The RMS values of I_1 and I_2 are calculated now independent of each other and are represented as 32-bit values (format +15.16).

  The RMS values of I_1 and I_2 are now calculated using apparent power and the RMS value of V1. See section “IRMS” for details.

- If voltage $V_1$is disconnected and a supply voltage is still provided to the ESP430CE1A, the RMS values of I_1 and I_2 are calculated using the root mean square of the measured current samples. This allows the CPU to calculate an energy value with a nominal voltage value for V_1.

- The calculated dc offsets for I_1, I_2 .and V_1 are not cleared when the ESP430CE1A comes out of Idle mode.

- The influence of the voltage ADC to the two current ADCs can be eliminated by a selectable hardware-specific value at address CMRRCOMP. If it is zero, no common mode correction is used. Additionally, the flag I2CMRR in register ESP430_CTRL0 can switch off the correction for current path I2. For details, see section “Common Mode Rejection Ratio”.

- Interrupts are generated for both positive and negative energies and is indicated by the flag ILNEGFG.

1.2 ESP430CE1(A) Operation

The ESP430CE1(A) module is configured with user software. The setup and operation of the ESP430CE1(A) is discussed in the following sections.

1.2.1 ESP430 Operation and Access

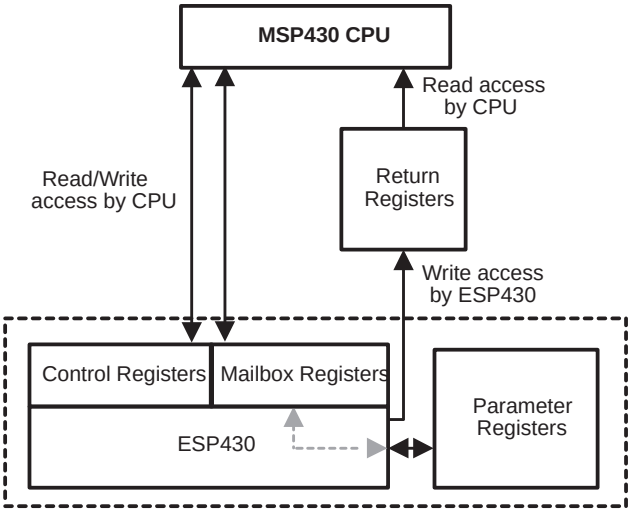
The ESP430 controls the analog sampling of the module and performs the metering calculations in parallel to CPU activity. This includes dedicated access to the SD16 and hardware multiplier modules when the ESP430 is enabled. In this case, the CPU cannot control or access the SD16 or the hardware multiplier.

Note: Suspending the ESP430

The ESP430 can be suspended by setting ESPSUSP in ESPCTL. Once ESPSUSP = 1, a delay of 9 MCLK cycles are required prior to the CPU accessing the SD16 or hardware multiplier modules.

ESP430 setup, control and access is provided by accessing data and control registers. These registers fall into three categories: control and mailbox registers, parameter registers, and return registers. Figure 1−2 shows the communication links connecting each category with the ESP430 and CPU.

Figure 1−2. Module Control and Value Access Registers

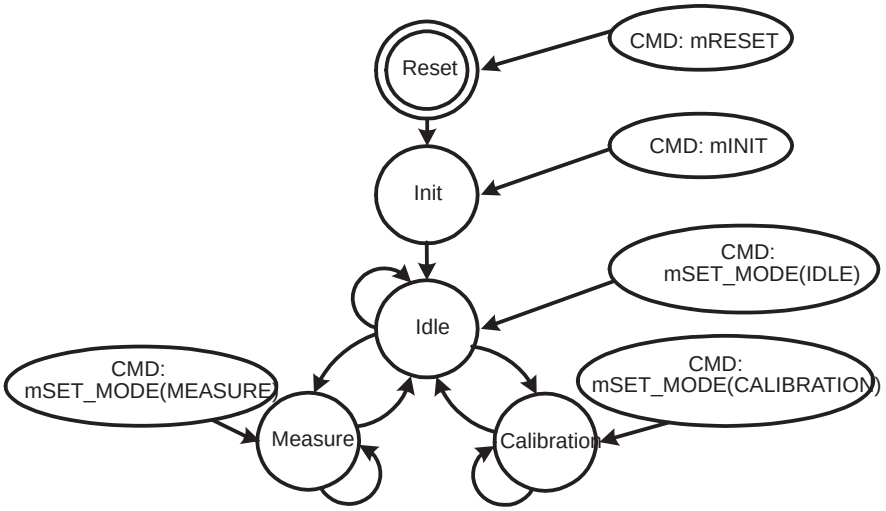


The CPU controls the operation of the ESP430 which in turn controls the analog sampling and data processing of the metering analog front-end. The ESP430 also performs all parameter calculations such as active energy, apparent energy, power factor, etc. Operation of the ESP430 is performed using the ESPCTL register.

1.2.2 ESP430 Modes of Operation

The ESP430 operating modes are shown in Figure 1−3.

Figure 1−3. ESP430 Operational State Diagram



Modes are entered through commands sent by the CPU. These commands are transmitted to the ESP430 using the mailbox communication architecture. These modes are defined in Table 1−1.

Table 1−1. ESP430 Operational Mode Summary

Mode	Command	Function
RESET	mRESET	ESP430CE1 module is reset: − Parameter registers are initialized − Return registers are cleared Upon completion, INIT mode is entered.
INIT	mINIT	Internal offset calibration of the AFE is performed. Offset of each SD16 channel is measured and stored using the shunted ADC input. Upon completion, the IDLE mode is entered.
IDLE	mSET_MODE(IDLE)	Operation of the ESP430 is halted. The following actions are performed in IDLE mode before halt: − Status bits in ESP430_STAT0 are cleared − SD16 conversions are stopped − ESP430 data processing is stopped IDLE mode is exited by CPU-issued command. ESP430CE1: the RAM is cleared completely. ESP430CE1A: the RAM is cleared with the exception of the dc offset registers for I1, I2 and V1. This allows fast return to full accuracy of the ADCs.
MEASURE	mSET_MODE (MEASURE)	SD16 conversions active; all metering calculations are performed continuously and written to the Return registers. IDLE mode is exited by CPU-issued command.
CALIBRATION	mSET_MODE (CALIBRATION)	Calibration of analog front-end and all meter parameters active. Used during production for the purpose of calibrating meter-specific performance and constants. Upon completion, IDLE mode is entered.

1.2.3 ESP430CE1(A) Mailbox Communication

The CPU communicates with the ESP430 via the mailbox register architecture. Incoming (ESP430 to CPU) and outgoing (CPU to ESP430) mailboxes are used to control the operation of the ESP430 and for access to Parameter registers. Three groups of mailbox commands are implemented:

− Control Commands: Request defined action of the ESP430 (Outgoing)
− Parameter Commands: Modify Parameter register values (Outgoing)
− Return Commands: Acknowledge or Notification by the ESP430 (Incoming)

A total of four 16-bit registers support incoming messages (MBIN0, MBIN1) and outgoing messages (MBOUT0, MBOUT1). The use of each mailbox register is described in the following sections.

Control Commands

Mailbox control commands are sent by the CPU and define actions to be performed by the ESP430. Table 1−2 lists the available control commands.

Table 1−2. Mailbox Control Commands

Control Command	MBOUT0 Value		MBOUT1 Value	Description
	ESP430CE1	ESP430CE1A		
mRESET	0001h	0001h	N/A	ESP430 enters RESET mode. No acknowledge is returned to the CPU.
mSET_MODE	0003h	0003h	0:IDLE 2:CALIBRATION 4:MEASURE 6:RESET 8:INIT	ESP430 enters specified mode. No acknowledge is returned to the CPU. RESET and INIT can also be entered by using commands mRESET and mINIT, respectively.
mCLR_EVENT	0005h	0005h	16-bit value specifying event flags to be cleared	Flags are cleared in ESP430_STAT0.
mINIT	0007h	0007h	N/A	ESP430 enters INIT mode. No acknowledge is returned to the CPU.
mTEMP	0009h	0009h	N/A	Request integrated temperature measurement. ESP430 returns mTEMPRDY in MBIN0 and conversion result in MBIN1.

Table 1−2. Mailbox Control Commands (continued)

Control Command	MBOUT0 Value		MBOUT1 Value	Description
	ESP430CE1	ESP430CE1A		
mSWVERSION	000Bh	000Bh	N/A	Request ESP430 firmware version. ESP430 returns mSWRDY in MBIN0 and version value in MBIN1. The ESP430 expects the CPU to accept an immediate mail return after the mSWVERSION command is issued.
mREAD_PARAM	000Dh	000Dh	Address value of parameter register to be read. See Table 1−3 for a complete list of Parameter registers and their address values.	Read Parameter register. ESP430 returns mPARAMRDY in MBIN0 and the Parameter register value in MBIN1. The ESP430 expects the CPU to accept an immediate mail return after the mREAD_PARAM command is issued.
mI2	000Fh	000Fh	N/A	Single measurement on I2 channel
mI2_CONT	N/A	0011h	N/A	Continuous measurement on I2 channel
mLOAD_PC	0011h	0013h	Start address of called subroutine	
mSET_RES_SC	N/A	0015h	N/A	For test purposes only

Note: Clearing ESP430_STAT0 Event Flags with mCLR_EVENT

Not all flags can be reset by the CPU due to independent activity by the ESP430. These flags include I2GTI1FG, ZXLDFG, ZXTRFG, and ACTIVEFG. See the description of the individual flags for details.

Temperature Measurement and the ESP430

A temperature measurement is triggered with the mTEMP command sent to the ESP430. With the next zero crossing of the signal on V_1, an internal temperature measurement is performed. Upon completion, the mTEMPRDY command is returned in MBIN0 along with the 16-bit result in MBIN1. The temperature is calculated using the equation given below.

$$T\,[^{o}C] = (\text{MBIN1}) \times \frac{V_{REF}\,[V] \times 1000}{65535 \times T_C\,[mV/K]} - \frac{V_{OFFSET}\,[mV]}{T_C\,[mV/K]} - 273\,[^{o}C]$$

The parameters T_C and V_{OFFSET} refer to the temperature sensor. See the device-specific data sheet for more information.

Parameter Commands

The parameter commands are used by the CPU to access the ESP430 Parameter registers. Refer to the Parameter Register Summary section for detailed description of each Parameter register value. Table 1−3 lists each parameter command. In each instance, MBOUT1 contains the data value to be written to the specified Parameter register and is not shown.

Table 1−3. Mailbox Parameter Commands

Parameter Command	Target Register	MBOUT0 Value Register Pointer
mSET_CTRL0	ESP430_CTRL0	0200h
mSET_CTRL1†	ESP430_CTRL1	0202h
mSET_EVENT	EVENT	0204h
mSET_PHASECORR1	PHASECORR1	0206h
mSET_PHASECORR2	PHASECORR2	0208h
mSET_V1OFFSET	V1OFFSET	020Ah
mSET_I1OFFSET	I1OFFSET	020Ch
mSET_I2OFFSET	I2OFFSET	020Eh
mSET_ADAPTI1	ADAPTI1	0210h
mSET_ADAPTI2	ADAPTI2	0212h
mSET_GAINCORR1	GAINCORR1	0214h
mSET_POFFSET1_LO	POFFSET1_LO	0216h
mSET_POFFSET1_HI	POFFSET1_HI	0218h
mSET_GAINCORR2	GAINCORR2	021Ah
mSET_POFFSET2_LO	POFFSET2_LO	021Ch
mSET_POFFSET2_HI	POFFSET2_HI	021Eh
mSET_INTRPTLEVL_LO	INTRPTLEVL_LO	0220h
mSET_INTRPTLEVL_HI	INTRPTLEVL_HI	0222h
mSET_CALCYCLCNT	CALCYCLCNT	0224h
mSET_STARTCURR_FRAC	STARTCURR_FRAC	0226h
mSET_STARTCURR_INT	STARTCURR_INT	0228h
mSET_NOMFREQ	NOMFREQ	022Ah
mSET_VDROPCYCLS	VDROPCYCLS	022Ch
mSET_RATIOTAMP	RATIOTAMP	022Eh
mSET_ITAMP	ITAMP	0230h
mSET_VDROPDLEVEL	VDROPDLEVEL	0232h
mSET_VPEAKLEVEL	VPEAKLEVEL	0234h
mSET_IPEAKLEVEL	IPEAKLEVEL	0236h
mSET_DCREMPER	DCREMPER	0238h
mSET_DELTAV1MAX†	DELTAV1MAX	023Ah
mSET_CMRRCOMP†	CMRRCOMP	023Ch
mSET_FADCU†	FADCU	023Eh

† A Parameter command will overwrite any existing value in the register with the new value passed in MBOUT1. The ESP430 will return the command mPARAM_SET in MBIN0 and the requested Parameter register pointer value in MBIN1 after the register is updated. Present only in the ESP430CE1A.

Return Commands

The mailbox return commands notify the CPU that the ESP430 has completed an action or that an event has occurred. Table 1−4 lists the ESP430 return commands. Refer to the Control and Parameter Command sections for more information.

Table 1−4. Mailbox Return Commands

Return Command	MBIN0 Value	MBIN1 Value	Description
mPARAM_SET	0009h	16-bit Parameter register pointer value (see Table 1−3)	Acknowledge a parameter register was modified and notify CPU
mPARAMRDY	0007h	16-bit Parameter register data value	Acknowledge a parameter register was queried and return value to CPU
mSWRDY	0005h	ESP430 revision number	Acknowledge revision was queried and return revision number to CPU
mTEMPRDY	0003h	16-bit temperature conversion result	Acknowledge a temperature measurement was requested and return result to CPU
mEVENT	0001h	16-bit ESP430_STAT0 value (Refer to the ESP430_STAT0 register description)	Notify CPU that an enabled event has occurred and return ESP430_STAT0 value to the CPU

1.2.4 Sampling Rate

The AFE sampling rate is the modulator input frequency divided by the oversampling ratio: $f_{ADC} = f_M$ /SD16OSRx. If not otherwise noted, the sampling rate of f_{ADC} = 1.048576 MHz / 256 = 4096 Hz has been assumed.

Note: SD16OSRx Settings

The SD16OSRx settings for each SD16 channel must be identically configured for proper ESP430 operation. Failure to assign the same oversampling rate to all SD16 channels will cause erroneous ESP430 calculation results.

The number of samples for a complete ESP430 calculation sequence is 4096 and is independent of f_{ADC}. The measurement time for a complete measurement sequence is based on f_{ADC}. The sampling period is divided into 256 units to get the time base unit for the ESP430.

$$\text{ESP430 timebase unit} = \frac{1}{f_{ADC} \times 256}$$

All timings are expressed with this unit and some common values are given in Table 1−5.

Table 1−5. ESP43 Timebase and ADC Repetition Frequencies

f_{ADC}	ESP430 Timebase Unit	Measurement Time	Minimum MCLK Frequency
4096 Hz	953.674 ns (2^{-20} s)	1.0 s	4.194 MHz
2048 Hz	1.907348 µs (2^{-19} s)	2.0 s	2.097 MHz
1024 Hz	3.814697 µs (2^{-18} s)	4.0 s	1.049 MHz

The minimum MCLK frequency for the ESP430 is dependent upon the desired ESP430 functions to be performed and f_{ADC}. Table 1−6 shows the minimum MCLK frequency for ESP430 function combinations.

Table 1−6. Minimum MCLK Frequency (SD16OSRx = 256)

Enabled Functions	Minimum SD16DIVx	MCLK Minimum Frequency (per ADC sampling rate, f_{ADC})		
		1024 Hz	*2048 Hz*	*4096 Hz*
Measure I_1	10b: /4	2 MHz	4 MHz	8 MHz
Measure I_1 and I_2	10b: /4	2 MHz	4 MHz	8 MHz
Measure I_1 and I_2 Enable DC removal function	10b: /4	2 MHz	4 MHz	8 MHz
Measure I_1 and I_2 Correct for DC tolerant CTs	11b: /8	2.27 MHz	4.4 MHz	8.39 MHz
V_1 filter enabled		2.2 MHz	4.4 MHz	8.39 MHz
All functions enabled	11b:/8	2.2 MHz	4.4 MHz	8.39 MHz

For reduced power consumption of the ESP430CE1, f_{ADC} can be reduced. This change effects the meter-specific constants which must be modified accordingly. With a lower f_{ADC}, the MCLK frequency can be reduced with all functions remaining enabled.

Note: SD16 Clock Source and Low Power Modes

When the CPU enters low power modes, the clock source to the SD16 must not be disabled during ESP430 operation. Turning off the SD16 clock source will halt ADC conversions and ESP430 operation will halt. User software must account for this operation when low power modes are used.

1.2.5 Reasons for False Measurements

If the ESP430CE1(A) shows false measurements, the following reasons are possible:

- ❑ The external hardware is erroneous (open and wrong connections, failures).
- ❑ The MCLK frequency of the ESP430CE1(A) is too low. See previous tables for the minimum MCLK frequencies.
- ❑ The ADC clock f_{ADC} that is in use is too high for the MCLK frequency.
- ❑ The measured values for V_1, I_1, and I_2 are > 7FFFh (+32767) or < 8000h (−32768). The ADC delivers the saturated values 7FFFh or 8000h. A hardware check is necessary.
- ❑ The values for (ADAPTI1) or (ADAPTI2) are too high. The multiplication with the ADC values for V_1, I_1, and I_2 deliver the saturated values 7FFFh or 8000h.
- ❑ The V1FILTER is enabled with a too low value for (DELTAV1MAX). Too many approximated V_1 samples are used for the calculations.

1.2.6 ESP430 Energy Measurement Configurations

The ESP430 can operate in two different energy measurement configurations which are summarized in Table 1−7.

Table 1−7. Measurement Configuration Summary

Configuration	Description
Energy Measurement using I_1 only (2-wire or 3-wire meter architecture)	Line voltage and current using V_1 and I_1 are measured. I_2 not used externally and is reserved for temperature measurement. Limited tamper-detection capability is available: − Disconnection of the Mains Voltage − Reversed Meter Connections I2GTI1FG and TAMPFG always = 0
Energy plus Tamper Detection Measurement using I_1 and I_2 (2-wire meter architecture only)	Line voltage and current using V_1 and I_1 are measured. I_2 is used to measure neutral current enabling full tamper-detect capability: − Disconnection of the Mains Voltage − Reversed Meter Connections − Earthing of the Load Temperature measurement is performed by I_x channel and is automatically selected by the ESP430.

Note: Tamper Detection and ADAPTx Parameter Registers

When the energy plus tamper detect configuration is used, it is necessary to adapt the meter constants C_{Z1} and C_{Z2} using the Parameter registers ADAPT1 and ADAPT2. See the specific Parameter register descriptions for more information.

Disconnection of the Mains Voltage

This condition occurs when voltage connections of the electricity meter are removed. With a coil around the current path providing a supply voltage to the MSP430, basic meter functionality can continue. The CPU must sample the current channel using the SD16 directly and perform the required calculations in order to continue accumulating energy. The missing voltage value can be replaced by the highest specified mains voltage for the system. The ESP430 should be disabled to minimize current consumption.

Reversed Meter Connections

This condition occurs when either the voltage or the current connections of the electricity meter – but not both – are reversed. It is indicated when ACTENERGY1 contains a negative energy value. The CPU must define the treatment of negative active energy values calculated by the ESP430 and take appropriate action when negative active energy is encountered. The treatment of negative active energy by the ESP430 is defined by NE1 and NE0 in ESP430_CTRL0 and is defined in Table 1−8.

Table 1−8. ESP430 Treatment of Negative Active Energy

NE1	NE0	ESP430 Action
0	0	Energy not summed, active energy is set to zero, NEGENFG = 1
0	1	Absolute active energy is summed, NEGENFG = 1
1	0	Negative active energy is summed, NEGENFG = 1 Return register POWERFCT is negative
1	1	Reserved

Earthing of the Load

This condition occurs when the load is not connected to the neutral return but to an earth ground connection. This is potentially the case when I_1 has a significantly larger value than I_2 (or vice-versa) and depends on the electricity meter circuitry. The CPU must use the provided energy values and take appropriate action.

Comparison of two Currents

Fundamental operation of the complete tamper detection features of the ESP430 require a comparison of currents on both I_1 and I_2. The ESP430 measures the meter current at I_1 and I_2 when both channels are used and the larger of the two RMS values is used for all calculations.

I2GTI1FG in Return register ESP430_STAT0 indicates the channel measuring the greater current:
− I2GTI1FG = 0: $I_1 \geq I_2$. Current I_1 is used
− I2GTI1FG = 1: $I_1 < I_2$. Current I_2 is used

TAMPFG in Return register ESP430_STAT0 indicates if tampering (defined by Parameter register RATIOTAMP) occurred during the last measurement period (4096 samples). RATIOTAMP defines the percentage difference between both I_x channels allowed before a possible tampering condition is indicated (0% to 100%: $1.0 \leq \langle RATIOTAMP) \times 2^{-14} < 2.0$).

TAMPFG = 0: no tampering detected
− I2GTI1FG = 0: $I_1 < I_2 \times \langle RATIOTAMP) \times 2^{-14}$
− I2GTI1FG = 1: $I_2 < I_1 \times \langle RATIOTAMP) \times 2^{-14}$

TAMPFG = 1: possible tampering condition
− I2GTI1FG = 0: $I_1 \geq I_2 \times \langle RATIOTAMP) \times 2^{-14}$
− I2GTI1FG = 1: $I_2 \geq I_1 \times \langle RATIOTAMP) \times 2^{-14}$

The tampering check threshold for each channel is defined by the ITAMP Parameter register. If the RMS values of I_1 and I_2 are lower than the tamper threshold current provided, the tamper check calculations are not performed and TAMPFG = 0.

1.2.7 Meter Constants and the ESP430

The ESP430 processes AFE conversion data and calculates the Return register results. With user software, the CPU calculates meter-specific values for voltage, current, energy, power, etc. from the relative values provided by the ESP430. In order to calculate the meter-specific values from the relative values provided by the ESP430, meter constants must be defined.

The meter constant C_Z is given by:

$$C_Z = \frac{f_{ADC}}{k_V \times k_I \times 4096} \left[\frac{steps^2}{Ws}\right]$$

When f_{ADC} = 4096Hz this simplifies to:

$$C_Z = \frac{1}{k_V \times k_I \times 1sec} \left[\frac{steps^2}{Ws}\right]$$

The variables k_V and k_I represent the meter-specific constants used by the CPU to calculate actual voltages and currents from the values of the Return registers. Different constants can exist for each current path and are differentiated by a 1 or 2 for I_1 and I_2, respectively, where appropriate. Return value equations used by the ESP430 and meter-specific relationships used by the CPU are described in the following sections.

Note: Equations and ESP430 Registers

Throughout this document, equation variables enclosed in “( )” refer to values contained in ESP430 Parameter or Return registers.

1.2.8 ESP430CE1 Parameter Register Description

The Parameter registers contain information provided by the CPU that controls how the ESP430 processes the current and voltage sample data.

The Parameter registers are located within the ESP430 and are accessed using the mailbox communication registers. The following section describes each Parameter register.

ESP430_CTRL0: ESP430 Control Register 0

The ESP430_CTRL0 register controls the calculation functionality of the ESP430 and is described in Table 1−9.

Table 1−9. ESP430_CTRL0 Summary

Name	Bit Function
CURR_I2	CURR_I2 enables the external use of analog channel I_2. − CURR_I2 = 0: I_2 is disabled and not used externally − CURR_I2 = 1: I_2 accepts a connection to a current transformer (CT), DC-tolerant CT or shunt sensor for tamper detection operation.
CURR_I1	CURR_I1 enables the external use of analog channel I_1. − CURR_I1 = 0, I_1 accepts a connection to a CT, DC-tolerant CT or shunt sensor for measurement of the line current − CURR_I1 = 1: Reserved
MB	MB defines the operation ILREACHEDFG indicating that an interrupt level has been reached specified in the INTRPTLEVL Parameter register. − MB = 0: ILREACHEDFG is set after a defined accumulated energy level has been reached specified by INTRPTLEVL. The value in INTRPTLEVL is subtracted from the ESP430 energy sum and accumulation of energy continues. − MB = 1: ILREACHEDFG is set after a defined number of measurements has been completed specified by INTRPTLEVL. The ESP430 internal measurement counter is cleared and counting resumes from 0.
NE0 NE1	NEx bits define the ESP430 handling of a negative active energy result. Refer to Table 1−8 for additional information.
DCREM_V1 DCREM_I1 DCREM_I2	DCREM_xx enables the ESP430 DC removal functionality for measurements made on the respective AFE channel: V_1, I_1, or I_2. − DCREM_xx = 0: the removal function is disabled. ADC conversion values are corrected using the offset correction value obtained for the specific AFE channel during the INIT mode of the ESP430 startup operation. − DCREM_xx = 1: the removal function is enabled. ADC conversion values are corrected using the DC removal function.
V1FILTER	The V1FILTER Bit (bit 8) switches the spike filter function for the voltage V1. Implemented with the ESP430CE1A only.
I2CMRR	The CMRR Enable Bit (bit 9) switches the common mode rejection function for the current I2. Implemented with the ESP430CE1A only.

Note: Enabling DC Removal for Multiple AFE Channels

It is not necessary to enable DC removal for all channels, and it must be enabled only for the voltage path or the current path. When both I_1 and I_2 are used, and DC removal is required in the current path, the DC removal function can be enabled for both current channels as required by the measurement configuration.

DC Removal Bit for V_1 − DCREM_V1

The DCREM_V1 Bit (bit 5) switches the dc removal function for the voltage V1. A description of the dc removal is given in section “DC Removal Period Count”.

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DCREM_V1 = 0: The dc removal function for V_1 is switched off, the ADC offset N_{V1SC} measured with shorted ADC inputs for V1 is used instead.

DCREM_V1 = 1: The dc removal function for V_1 is switched on.

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DCREM_V1 = 0: The dc removal function for V_1 is switched off, an ADC offset 0 is used instead.

DCREM_V1 = 1: The dc removal function for V_1 is switched on.

DC Removal Bit for I1 − DCREM_I1

The DCREM_I1 Bit (bit 6) switches the dc removal function for the current I_1.

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DCREM_I1 = 0: The dc removal function for I_1 is switched off, the ADC offset N_{I1SC} measured with shorted ADC inputs for I_1 is used instead.

DCREM_I1 = 1: The dc removal function for I_1 is switched on. If a Rogowski coil is used (CURR_I1 = 1) the dc removal for the di/dt integrator is enabled, too.

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DCREM_I1 = 0: The dc removal function for I_1 is switched off, an ADC offset 0 is used instead.

DCREM_I1 = 1: The dc removal function for I_1 is switched on.

DC Removal Bit for I2 − DCREM_I2

The DCREM_I2 Bit (bit 7) switches the dc removal function for the current I_2.

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DCREM_I2 = 0: The dc removal function for I_2 is switched off, the ADC offset N_{I2SC} measured with shorted ADC inputs for I_2 is used instead.

DCREM_I2 = 1: The dc removal function for I_2 is switched on.

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DCREM_I2 = 0: The dc removal function for I_2 is switched off, an ADC offset 0 is used instead.

DCREM_I2 = 1: The dc removal function for I_2 is switched on.

Spike Filter Enable Bit for V_1 − V1FILTER

The V1FILTER Bit (bit 8) switches the spike filter function for the voltage V1. Implemented with the ESP430CE1A only.

V1FILTER = 0: No filter function. The V_1 input samples are not checked.

V1FILTER = 1: The spike filter function for V_1 is enabled. The absolute value of the difference $|N_{v1n} - N_{v1n-1}|$ is compared to the value contained in word DELTAV1MAX. If the absolute value of this difference is smaller, the original V_1 sample is used. If the difference is larger or equal, a linear approximation of the two previous V_1 values (N_{v1n-1}, N_{v1n-2}) is used instead for N_{v1n}. See section “Maximum Spike for V_1 Filter” for details.

CMRR Enable Bit for I_2 − I2CMRR

The CMRR Enable Bit (bit 9) switches the common mode rejection function for the current I_2. Implemented with the ESP430CE1A only.

I2CMRR = 0: No common-mode rejection function for I_2. This allows the use of current sensors with relatively high output voltages like current transformers.

I2CMRR = 1: The common-mode rejection function for I_2 is enabled, if the value in parameter register CMRRCOMP > 0. See section “Common Mode Rejection Ratio” for details.

EVENT: Event Message Enable Control Register

The message enable bits in EVENT enable a mEVENT mailbox message return command to be sent by the ESP430 to the CPU when the corresponding event occurs. An event is the setting of a previously cleared bit in the ESP430_STAT0 register. A static level of a flag in ESP430_STAT0 or resetting of a flag not previously cleared will not generate an event. The event flags in ESP430_STAT0 are set independently of the message enable settings.

PHASECORRx: I_X Phase Correction

PHASECORRx defines the phase correction for I_x where x = 1 or 2 for channels I_1 and I_2, respectively. The value specified is used for phase error correction of a simple or DC tolerant current transformer on I_x. If this value is non−zero, the correction calculations are made during the measurement process. If a shunt is used on I_x, set PHASECORRx = 0.

PHASECORRx > 0: I_x leads V_1 (capacitive characteristic of DC tolerant CTs)
PHASECORRx < 0: I_x lags V_1 (inductive characteristic of simple CTs)

Format	Signed integer	±15.0
Range	0x8000 to 0x7FFF	−31.25 ms to +31.2490 ms (f_{MAINS} = 50Hz, f_{ADC} = 4096Hz)
Normal Range	−2° to +8°: 0xFF8C to 0x01D2 (f_{MAINS} = 50Hz, f_{ADC} = 4096Hz)	−111 us to +444 us (f_{MAINS} = 50Hz, f_{ADC} = 4096Hz)
Resolution	ESP430 timebase unit	2^{-20} s (f_{ADC} = 4096Hz)
Initialization	0x00	

Formulas:

$$(\text{PHASECORRx}) = \frac{\varphi_{CT}}{360^o \times f_{MAINS(nom)}} \times \frac{1}{\text{ESP430 Timbase Unit}}$$

Example: The phase error, φ_{CT}, of a DC tolerant current transformer on I_1 is specified to be +4.2° at 50 Hz; f_{ADC} = 4096 Hz. The rounded value calculated for PHASECORR1 is:

$$(\text{PHASECORR1}) = \frac{4.2^o}{360^o \times 50\text{Hz}} \times \frac{1}{2^{-20}} = 244.667 \approx 0\text{x5F}$$

Example: A simple current transformer on I_1 has an inductive phase error of −1° at 50 Hz; f_{ADC} = 4096 Hz. The rounded value in PHASECORR1 is:

$$(\text{PHASECORR1}) = \frac{-1.0^o}{360^o \times 50\text{Hz}} \times \frac{1}{2^{-20}} = -58.254 \approx 0\text{xFFC6}$$

V1OFFSET: V_1 Offset Correction

V1OFFSET defines the ADC offset correction for V_1. The value specified is added to the ADC result in order to measure 0 when 0V is applied externally.

Format	Signed integer	±15.0
Range	0x8000 to 0x7FFF	−32,768 to +32,767
Normal Range	0xFE00 to 0x0200	±512
Resolution	1 step	
Initialization	0x00	

Formulas:

$$(\text{WAVEFSV1}) = N_{V1ADC} - N_{V1SC} + (\text{V1OFFSET})$$

Where:
N_{V1ADC}: Conversion value from SD16
N_{V1SC}: ESP430-corrected offset value

N_{V1SC} represents two different values dependent on DCREM_V1:

DCREM_V1 = 0: N_{V1SC} is the offset measured during the INIT mode of the ESP430 startup (internally shorted ADC input result)

DCREM_V1 = 1: N_{V1SC} is the offset resulting from the ESP430 DC removal calculation for V_1. V1OFFSET is not used and should be set to 0.

IxOFFSET: I_X Offset Correction

IxOFFSET defines the ADC offset correction for I_x where x = 1 or 2 for channels I_1 and I_2, respectively. The value specified is added to the ADC result in order to measure when 0A is applied to the shunt or CT externally for the respective I_x channel.

Format	Signed integer	±15.0
Range	0x8000 to 0x7FFF	−32,768 to +32,767
Normal Range	0xFE00 to 0x0200	±512
Resolution	1 step	
Initialization	0x00	

Formulas:

$$(\text{WAVEFSIx}) = \left(N_{IXADC} - N_{IXSC} + (\text{IxOFFSET})\right) \text{ x } (\text{ADAPTIx}) \text{ x } 2^{-14}$$

Where:
N_{IxADC}: Conversion value from SD16
N_{IxSC}: ESP430-corrected offset value

N_{IxSC} represents two different values dependent on DCREM_Ix:

DCREM_Ix = 0: N_{IxSC} is the offset measured during the INIT mode of the ESP430 startup (internally shorted ADC input result)

DCREM_Ix = 1: N_{IxSC} is the offset resulting from the ESP430 DC removal calculation for I_x. IxOFFSET is not used and should be set to 0.

ADAPTIx: I_x Adaptation Current

ADAPTIx defines the multiplication factor for the adaptation of the I_x ADC result. This parameter is used to provide equal current constants k_{I1} and k_{I2} (and therefore equal meter constants C_{Z1} and C_{Z2}) for the currents I_1 and I_2 despite possible hardware implementation differences. In order to assure that the meter constants can be adapted, I_1 and I_2 should be matched as close as possible using the AFE gain settings.

Format	unsigned Integer.Fraction	+1.14
Range	0x00 to 0x7FFF	0.0 to 1.999938965
Normal Range	0x2000 to 0x7FFF	0.5 to 1.999938965
Resolution	61.035×10^{-6}	2^{-14}
Initialization	0x4000	1.000

Formulas:

$$(\text{ADAPTIx}) = \frac{k_{Ix}}{k_{Icom}} \times 2^{14}$$

Where:
k_{Ix}: I_x meter constant
k_{Icom}: Common meter constant

Example: The I_1 meter constant should be modified to $k_{Icom} = 2.5 \times 10^{-3}$ from the actual meter constant $k_{I1} = 2.21946 \times 10^{-3}$. The rounded value required in ADAPTI1 is:

$$(\text{ADAPTI1}) = \frac{k_{I1}}{k_{Icom}} \times 2^{14} = \frac{2.21946 \times 10^{-3}}{2.5 \times 10^{-3}} \times 2^{14} = 0.887784 \times 2^{14} =$$

$$= 14,545.45306 \approx 0x38D1$$

Note: ADAPTIx Minimum Values

The I_1 ADC result WAVEFSI1 is corrected with the offset correction value I1OFFSET, the offset value N_{I1SC} which depends on DCREM_I1 and the value in ADAPTI1. It is recommended that $\text{ADAPT1} * 2^{-14} \geq 1$. Results less than 1 may degrade calculation accuracy. This also applies to ADAPTI2.

GAINCORRx: I_X Gain Correction

GAINCORRx defines the slope for the correction of the product WAVEFSV1*WAVEFSIx, where x = 1 or 2 for channels I_1 and I_2, respectively. Before internally summing the new value, the product of the new voltage and current samples is corrected with GAINCORRx and POFFSETx. Refer to "ESP430CE1A Calibration" for more information.

Format	unsigned Integer.Fraction	+1.14
Range	0x00 to 0x7FFF	0.0 to 1.999938965
Normal Range	0x3999 to 0x4666	1±10%
Resolution	61.035×10^{-6}	2^{-14}
Initialization	0x4000	1.000

Formulas:

$$(\text{GAINCORRx}) = \text{slope} \times 2^{14} = \frac{n_{HIcalc} - n_{LOcalc}}{n_{HImeas} - n_{LOmeas}} \times 2^{14}$$

Where:
n_{HIcalc}: Calculated result at the high current calibration point [steps^2]
n_{HImeas}: Measured result at the high current calibration point [steps^2]
n_{LOcalc}: Calculated result at the low current calibration point [steps^2]
n_{LOmeas}: Measured result at the low current calibration point [steps^2]

n_{LOcalc} and n_{LOmeas} are both zero for a single point calibration.

Example: Calibration resulted in a necessary gain correction of 1.0145 (slope). The value in GAINCORR1 is:

$$(\text{GAINCORR1}) = 1.0145 \times 2^{14} = 16,621.568 \approx 0x40EE$$

POFFSETx: I_x Power Offset Correction

POFFSETx (POFFSETx = POFFSETx_HI,POFFSETx_LO = 32-bit value) defines the offset for the correction of the product WAVEFSV1*WAVEFSIx, where x = 1 or 2 for channels I_1 and I_2, respectively. Before internally summing the new value, the product of the new voltage and current samples is corrected with GAINCORRx and POFFSETx. Refer to “ESP430CE1A Calibration” for more information.

Format	Signed integer	±31.0
Range	0x8000,0000 to 0x7FFF,FFFF	−2.14748E+9 to +2.14748E+9
Normal Range	0xFF00,0000 to 0x100,0000	$\pm 2^{24}$
Resolution	1 step[2]	

Formulas:

$$P_{Ix} = \frac{(\text{WAVEFSIx}) \times (\text{WAVEFSV1}) \times (\text{GAINCORRx})}{2^{14}} + (\text{POFFSETx})$$

Where:

P_{Ix}: Corrected internal ESP430 power calculation for channel I_x

Note: POFFSETx Value Format

POFFSETx values are expressed in the internal number format used by the ESP430. These values are 4096 times larger than the calculated energy contained in addresses ACTENERGY1 and ACTENERGY2. This is due to the adaptation of the energy to the meter constants C_{Z1} and C_{Z2}.

INTRPTLEVL: Energy Overflow Interrupt Level

INTRPTLEVL (INTRPTLEVL = INTRPTLEVL_HI, INTRPTLEVL_LO = 32-bits) defines the trigger threshold for setting ILREACHEDFG in ESP430_STAT0. MB controls how the ESP430 uses INTRPTLEVL.

MB = 0: ILREACHEDFG = 1 when the ESP430 accumulated energy count reaches the value in INTRPTLEVL. INTRPTLEVL is subtracted from the ESP430 accumulated energy count and accumulation resumes. ILREACHEDFG is set with the repetition frequency f_{IL}.

MB = 1: ILREACHEDFG = 1 when the number of ESP430 measurement cycles performed reaches the value in INTRPLEVL. The 32-bit measurement count contained in NMBMEAS is cleared and measurement counting restarts at 0.

Format	Unsigned integer	+32.0
Range	0x00 to 0x0FFFF,FFFF	0 to +4.294967E+9
Resolution	MB = 0: 1 step^2 MB = 1: 1 measurement	
Initialization	0x8000,0000	2.147483E+9

Formulas:

Interrupt level frequency:

$$f_{IL} = P\,[W] \times \text{Interrupt Rate}\,[1/Ws] = \frac{P \times 4096 \times C_Z}{(INTRPTLEVL)}$$

$$\text{Energy per pulse}\,[Ws] = \frac{1}{\text{Interrupt Rate}} = \frac{(INTRPTLEVL)}{4096 \times C_Z}$$

$$f_{IL(min)} = \frac{P \times 4096 \times C_Z}{0xFFFF,FFFF}$$

$$f_{IL(max)} = f_{ADC} \rightarrow (INTRPTLEVL)_{min} > \frac{P_{max} \times 4096 \times C_Z}{f_{ADC}}$$

$$\text{Error}_{fIL(max)} = \frac{1}{(INTRPTLEVL)_{min}} = \frac{f_{ADC}}{P_{max} \times 4096 \times C_Z}$$

Example: ILREACHEDFG is to be set with a mean repetition frequency of f_{IL} = 2kHz for a power P = 3kW. The I_1 meter constant of the meter is C_{Z1} = 29,322.81 steps^2/Ws:

$$(INTRPTLEVL) = \frac{3\,[kW] \times 4096 \times 29,322.81\,[steps^2/Ws]}{2\,[kHz]} =$$

$$= 180,159,344.6 \approx 0x0ABD,0370$$

Example: ILREACHEDFG is to be set after 8192 measurements. The value in INTRPTLEVL is 0x2000 (INTRPTLEVL_LO = 0x2000, INTRPTLEVL_HI = 0x0). ILREACHEDFG is set every 2s if f_{ADC} = 4096Hz.

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Works for both positive and negative energies and is indicated by the flag ILNEGFG.

Note: Return Register Updates

When the interrupt level is reached, only ILREACHEDFG is set; the update of the return registers is not affected.

CALCYCLCNT: Calibration Cycle Count

CALCYCLCNT defines the number of mains frequency periods used for calibration when the ESP430CE1 is set to Calibration Mode.

Format	Unsigned integer	+16.0
Range	0x00 to 0xFFFF	0 to 65,535
Normal Range	0x01 to 0x200	1 to 512
Resolution	1 mains period	
Initialization	0x64	100 mains periods

Example: The calibration cycle count required is determined to be 40 mains cycles. The value stored in CALCYCLCNT is 0x0028.

STARTCURR: Energy Measurement Start Current

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STARTCURR (STARTCURR = STARTCURR_INT.STARTCURR_FRAC = 32−bits) defines the current threshold at which energy accumulation is performed when the ESP430 is not in calibration mode. If the measured current's RMS value is below the threshold defined by STARTCURR, no energy is accumulated.

When both I channels are used, the greater current value of I_1 and I_2 is used and is indicated by I2GTI1FG. In this configuration, when one I_x value is above the STARTCURR threshold, energies for both channels are accumulated.

Format	Unsigned Integer.Fraction	+15.16
Range	0x0.0 to 0x07FFF.FFFF	0.0 to +32767.9999
Normal Range	0x00 to 0x666.C000	0 to 5.0 %
Resolution	±0.25 steps are used for the comparison	
Initialization	0x17.2A90	0.1 % × 0x7FFF × 0.707

Formulas:

$$(\text{STARTCURR}) = \frac{I_{START}}{k_{Icom}} \text{ x } 2^{16}$$

Example : The required start current for an electricity meter is 40 mA. The value for STARTCURR is:

$$(\text{STARTCURR}) = \frac{40\ [\text{mA}]}{2.21946\text{x}10^{-3}\ [\text{A/step}]} \text{ x } 2^{16} =$$

$$= 1,181,116.127 = 0\text{x}0012,05\text{BC}$$

Note: STARTCURR Comparison

The 16-bit value in STARTCURR_INT and the two MSBs in STARTCURR_FRAC are used for the I_x comparison. The remaining LSBs are ignored.

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The value in STARTCURR defines the current value for the start of the energy counting if the Operation Mode is not set to Calibration. Below this value all calculated energies (active energy, reactive energy and apparent energy) provided for the CPU are zero. The RMS value of the measured current I is used. For a better resolution the fractional part is also defined. For the comparison the (IRMS) value is used: the flag I2GTI1FG defines if the result for I1RMS or I2RMS was stored there.

Format	Unsigned Integer.Fraction	+15.16
Range	0x0.0 to 0x07FFF.FFFF	0.0 to +32767.9999
Normal Range	0x00 to 0x666.5999	0 to 5.0%
Resolution	All 32 bits are used for the comparison	
Initialization	0x17.45A1	$0.1\% \times 0x7FFF \times 0.707$

Formulas:

$$(IRMS) = \frac{\sqrt{(ACTENERGY1)^2 + (REACTENERGY)^2}}{(VRMS)} \text{ [steps]} \quad \text{if I2GTI1FG} = 0$$

$$(IRMS) = \frac{\sqrt{(ACTENERGY2)^2 + (REACTENERGY)^2}}{(VRMS)} \text{ [steps]} \quad \text{if I2GTI1FG} = 1$$

$$(STARTCURR) = \frac{I_{START}}{k_{Icom}} \times 2^{16}$$

Example 1: See Example for ESP430CE1.

Example 2: The required start current for an electricity meter is 40 mA. The value for STARTCURR is:

$$(STARTCURR) = \frac{I_{START}}{k_{I1}} \times 2^{16} = \frac{40\ [mA]}{2.21946x10^{-3}\ [A/step]} \text{ x } 2^{16} =$$

$$= 1,181,116.127 = 0x0012,05BC$$

The value for STARTCURR is 0x05BC (to LSBs at address STARTCURR) and 0x0012 (to MSBs at address STARTCURR + 2). All 16 bits (0x05BC) at the address STARTCURR are used for the comparison.

NOMFREQ: Nominal Mains Frequency

NOMFREQ defines the expected nominal line, or mains, frequency. The mains frequency is required for ESP430 phase correction of DC tolerant current transformers using PHASECORRx.

Format	Unsigned Integer	+8.0
Range	0x00 to 0x0FF	0 to +255
Normal Range	0x28 to 0x46	40 to 70 Hz
Resolution	1 Hz	
Initialization	0x32	50 Hz

Example: The expected mains frequency is 60 Hz corresponding to NOMFREQ = 0x3C.

VDROPCYCLS: Voltage Drop Detection Cycles

VDROPCYCLS defines the maximum number of contiguous mains voltage cycles having an absolute peak value less than the threshold defined by VDROPLEVEL. If the number of low voltage mains voltage cycles reaches the VDROPCYCLS, VDROPFG in ESP430_STAT0 is set. VDROPFG is reset when the absolute peak level of the voltage is greater than the value in VDROPLEVEL.

Format	Unsigned Integer	+8.0
Range	0x00 to 0x0FF	0 to +255 mains periods
Normal Range	Full range	
Resolution	1 mains period	
Initialization	0x05	5 mains periods

Formulas:

$$\text{If } |(\text{WAVESFSV1})| \geq (\text{VDROPLEVEL}) : \text{VDROPFG} = 0, \text{vdrop}_{cnt} = 0$$

$$\text{If } |(\text{WAVESFSV1})| < (\text{VDROPLEVEL}) : \text{vdrop}_{cnt} = \text{vdrop}_{cnt} + 1$$

$$\text{If vdrop}_{cnt} \geq (\text{VDROPCYCLS}) : \text{VDROPFG} = 1$$

RATIOTAMP: Tampering Current Ratio

RATIOTAMP defines the threshold for the ratio of the internal ESP430 currents I_{1RMS} and I_{2RMS} used to indicate potential meter tampering. This feature is valid for the Energy Plus Tamper Detection configuration only. Both RMS currents are calculated and the greater of the two is stored in IRMS. TAMPFG in ESP430_STAT0 is set according to the comparison and depends on I2GTI1FG:

TAMPFG = 0: (no tampering) when:
− I2GTI1FG = 0:$I_{1RMS} < I_{2RMS} \times (\text{RATIOTAMP}) \times 2^{-14}$
− I2GTI1FG = 1: $I_{2RMS} < I_{1RMS} \times (\text{RATIOTAMP}) \times 2^{-14}$

TAMPFG = 1: (potential tampering occurred) when:
− I2GTI1FG = 0: $I_{1RMS} \geq I_{2RMS} \times (\text{RATIOTAMP}) \times 2^{-14}$
− I2GTI1FG = 1: $I_{2RMS} \geq I_{1RMS} \times (\text{RATIOTAMP}) \times 2^{-14}$

When hardware implementations for I_1 and I_2 vary, adaptation for the two channels may be required in order to get equivalent results under equivalent excitation. Refer to the ADAPTI1 and ADAPTI2 sections for more information.

Format	Unsigned Integer.Fraction	+1.14
Range	0x4000 to 0x7FFF	1.0 to +1.999938965
Normal Range	Full range	
Resolution	61.035×10^{-6}	2^{-14}
Initialization	0x4000	1.000

Formulas:

$$(\text{RATIOTAMP}) = \left(\frac{I_{HI}}{I_{LO}}\right)_{MAX} \times 2^{14}$$

Where:
I_{HI}: Larger RMS value of I_{1RMS} and I_{2RMS}
I_{LO}: Smaller RMS value of I_{1RMS} and I_{2RMS}

Example: When I_x RMS currents differ by more than 5 %, potential tampering has occurred. RATIOTAMP is:

$$(\text{RATIOTAMP}) = \left(\frac{1.05}{1.00}\right) \times 2^{14} = 17,203.2 \approx 0x4333$$

Note: I_x RMS Results and TAMPFG

When IRMS is less than the threshold set in ITAMP, TAMPFG = 0 and will not be set regardless of the measured RMS ratio for I_1 and I_2.

ITAMP: Tampering Current Threshold

ITAMP defines the RMS current threshold for I_1 and I_2 enabling the ESP430 to perform a tampering check using RATIOTAMP. This feature is valid for the Energy Plus Tamper Detection configuration only.

Format	Unsigned Integer	+15.0
Range	0x00 to 0x07FFF	0.0 to +32,767
Normal Range	Full range	
Resolution	1 step	
Initialization	0x2E	$0.2\ \% \times 0x7FFF \times 0.707$

Formulas:

$$(\text{ITAMP}) = \frac{I_{TAMP}}{k_{Icom}}$$

Where:
I_{TAMP}: Current threshold for tamper check
k_{Icom}: Common meter constant

Example: No tampering check to be made below 2% of the specified 40 A maximum RMS current for the meter. k_{Icom} = 0.0025 A/step. ITAMP is:

$$(\text{ITAMP}) = \frac{40 \times 0.02}{0.0025} = 320.0 = 0x140$$

VDROPLEVEL: Voltage Drop Detection Threshold Level

VDROPLEVEL defines the minimum absolute peak value of the mains voltage V_1 expected during a normal mains period. If VDROPLEVEL is not reached, an internal ESP430 counter increments. When this counter reaches the value in VDROPCYCLS, VDROPFG = 1.

Format	Unsigned Integer	+15.0
Range	0x00 to 0x07FFF	0.0 to +32,767
Normal Range	Full range	
Resolution	1 step	

Formulas:

$$(\text{VDROPLEVEL}) = \frac{|V_{1PEAK}|}{k_{V1}} = \frac{|V_1| \times \sqrt{2}}{k_{V1}} \quad \text{(for sinusoidal voltage)}$$

Example: VDROPFG should be set when V_1 falls below 75% of the nominal voltage of 230 V for 6 or more mains periods, $k_{V1} = 15.365513 \times 10^{-3}$. VDROPCYCLS = 0x6, VDROPLEVEL is:

$$(\text{VDROPLEVEL}) = \frac{|230 \times 0.75| \times \sqrt{2}}{15.365513 \times 10^{-3}} = 15,876.58 \approx 0x3E05$$

Note: VDROPFG and V1RMS

When V1RMS is less than 0.088*VDROPLEVEL, VDROPFG will be set independent of the internal ESP430 counter used for VDROPLEVEL.

VPEAKLEVEL: Voltage Peak Level

VPEAKLEVEL defines the maximum value for V_1. If the absolute value of the measured voltage is greater than VPEAKLEVEL, V1PEAKFG = 1, otherwise V1PEAKFG = 0. To filter out single spikes on the line, three contiguous measurements must exceed VPEAKLEVEL.

Format	Unsigned Integer	+15.0
Range	0x00 to 0x07FFF	0.0 to +32,767
Normal Range	Full range	
Resolution	1 step	
Initialization	0x7FFF	Maximum voltage value

Formulas:

$$(\text{VPEAKLEVEL}) = \frac{|V_{1MAX}|}{k_{V1}}$$

Where V_{1MAX}: Maximum V_1 peak voltage

Example: V_{1MAX} is specified to be ±398V; $k_{V1} = 15 \times 10^{-3}$. VPEAKLEVEL is:

$$(\text{VPEAKLEVEL}) = \frac{|V_{1MAX}|}{k_{V1}} = \frac{398[V]}{15 \times 10^{-3}\,[V/step]} \approx 0x67A5$$

V1PEAKFG = 1 if three contiguous, voltage samples greater than 0x67A5 or less than 0x985B are measured (0x985B = −0x67A5), else V1PEAKFG = 0.

IPEAKLEVEL: Current Peak Level

IPEAKLEVEL defines the maximum value for I_1 and I_2. If the absolute value of each measured current is greater than IPEAKLEVEL, IxPEAKFG = 1, otherwise IxPEAKFG = 0, where x = 1 or 2 for I_1 or I_2, respectively. To filter out single spikes on the line, three contiguous measurements must exceed IPEAKLEVEL.

Format	Unsigned Integer	+15.0
Range	0x00 to 0x07FFF	0.0 to +32,767
Normal Range	Full range	
Resolution	1 step	
Initialization	0x7FFF	Maximum current value

Formulas:

$$(\text{IPEAKLEVEL}) = \frac{|I_{max}|}{k_{Icom}}$$

Example: I1PEAKFG = 1 when a current sample greater than 42A*1.414 (peak value for 42A) is measured on I_1, k_{Icom1} = 0.0025 A/step. IPEAKLEVEL is:

$$(\text{IPEAKLEVEL}) = \frac{\left|42 \text{ x } \sqrt{2}\right|}{2.5\text{x}10^{-3}\left[\text{A/step}\right]} = 23,758.79 \approx \text{0x5CCE}$$

DCREMPER: DC Removal Period Count

DCREMPER defines the number of mains periods used for one iteration of the DC removal algorithm. Larger values in DCREMPER may improve noise suppression and result in longer calculation settling times. When the DC removal function is disabled, DCREMPER is not used.

If the dc removal function is not switched on (with bits DCREM_V1, DCREM_I1, DCREM_I2):

ESP430CE1: The offset measured with shorted ADC inputs during the initialization (or with the INIT Control Command) is used.

ESP430CE1A: The value 0 is used.

Format	Unsigned Integer	+6.0
Range	0x00 to 0x032	0 to +50 (due to 32-bit sum buffer capacity)
Resolution	1 mains period	
Initialization	0x05	5 mains periods

DC Removal Function Description

If the AFE voltage and current samples contain offsets or DC components, the measured energy W is:

$$W = \frac{1}{f_{ADC}} \times \sum_{t=0}^{t=\infty} (v_n + v_{dc}) \times (i_n + i_{dc}) =$$

$$= \frac{1}{f_{ADC}} \times \sum_{t=0}^{t=\infty} (v_n \times i_n + v_n \times i_{dc} + i_n \times v_{dc} + i_{dc} \times v_{dc})$$

Where:
v_{dc} = DC part of a voltage sample [V]
i_{dc} = DC part of a current sample [A]
v_n = voltage sample [V]
i_n = current sample [A]

NOTE: With the ESP430CE1A, a watchdog is implemented for a missing voltage V_1. See section “Zero Crossing watchdog”.

The terms $(v_n \times i_{dc})$ and $(i_n \times v_{dc})$ in the above equation equal zero when summed over one full mains period (the integral of a sine wave from 0 to $2\pi = 0$). However the term $(i_{dc} \times v_{dc})$ is added erroneously to the energy summation with each sample result. If one of the two offsets can be set to zero, the error term is eliminated.

With the DC removal function enabled, it is possible to eliminate the DC component for the V_1 voltage path or the current paths, I_1 and I_2. DCREMPER defines the number of mains periods used for the calculation of the DC removal values.

1.2.9 Detection of Zero Crossing

Zero Crossing Checks

Zero crossing of the voltage V_1 is detected by the change of the sign of V_1 after two samples with the same sign:

- ❏ Leading edge: a positive V_1 sample follows two negative ones.
- ❏ Trailing edge: a negative V_1 sample follows two positive ones.

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To get secure results with noise and spikes on the voltage V_1, two limits are given for the change of V_1:

- ❏ The two V_1 samples before and after the sign change must have minimum distances of 502 ADC steps. This avoids noise induced, false zero crossings.
- ❏ V1FILTER enabled: Spikes of V_1 are checked against the value (DELTAV1MAX) in the Parameter Registers. The voltage sample differences $|\Delta N_{v1}|$ must be smaller than (DELTAV1MAX), otherwise a linear approximation is used for the actual V_1 sample v1n.

The V1FILTER avoids false zero crossings by large spikes.

If V1FILTER = 0:

No V_1 check is made. Sample v1n is used as it is.

If V1FILTER = 1:

If $| N_{v1n} - N_{v1n-1} | < (DELTAV1MAX)$, sample v1n is used as it is.

Else $N_{v1n} = (N_{v1n-1} - N_{v1n-2}) + N_{v1n-1} = 2N_{v1n-1} - 2N_{v1n-2}$, a linear approximation for sample v1 is used.

If the V1FILTER is used, the value for (DELTAV1MAX) must be set by the CPU to the maximum dv1/dt value for the used ADC range, multiplied with a security factor k_{safety}, e.g., 1.2:

$$(DELTAV1MAX) = 2\pi \times f_{mains\,max} \times \frac{N_{ADC\,max}}{f_{ADC}} \times k_{safety}$$

Example: The V1FILTER is used with a used ADC range of 90 %, a maximum mains frequency of 51 Hz, an ADC frequency of 4096 Hz and a safety factor 1.1. The value in DELTAV1MAX is:

$$(DELTAV1MAX) = 2\pi \times 51 \times \frac{0.9 \times 7FFFh}{4096} \times 1.1 = 2538$$

Zero Crossing Watchdog (ESP430CE1A Only)

With V1 disconnected, no zero crossings occur and no mains period measurements are made. To allow the important dc removal calculations without V1, a watchdog is implemented for the zero crossing detection. This Zero Crossing Watchdog is reset with each detected valid zero crossing of V1 and incremented with the sample frequency f_{ADC}. If the watchdog reaches the fixed value:

$$ZCWD = \frac{f_{ADC\,max}}{f_{mains\,min}} + k_{ZCWD} = \frac{4096}{40} + 40 \simeq 142$$

the dc removal calculations are processed with the accumulated values and the watchdog is reset.

The maximum repetition frequency $f_{DCRmmax}$ of the dc removal function due to the Zero Crossing Watchdog is:

$$f_{DCRm\,max} = \frac{f_{ADC}}{(DCREMPER) \times ZCWD} + 1\ [Hz]$$

With the initial value of 5 for (DCREMPER) and f_{ADC} = 4096 Hz this leads to:

$$f_{DCRm\,max} = \frac{4096}{5 \times 142} + 1 \simeq 6\ [Hz]$$

The dc removal function is called with a repetition frequency of 6 Hz if V_1 is missing.

With the safety function of the Zero Crossing Watchdog, energy measurements are still possible without V1 connected: the correctly measured value IRMS is multiplied by a defined value for V_1, e.g., 100%. The multiplication and accumulation is made by the CPU in this case.

1.2.10 Common Mode Rejection (ESP430CE1A Only)

Figure 1−4 shows the common mode influence of the voltage V1 to the currents I1 and I2. This influence is only visible at very low currents. The common mode influence is a constant error value (shown red in the next figure) in phase with the voltage V1. The common mode influence changes the phase angle φ to φ' and the current values from I_1 and I_2 to I_1' and I_2' dependent on the quadrant of the current.

These two changes introduce a measurement error which depends on the phase angle φ and the current value.

Figure 1−4. Common-Mode Influence to the Current Path

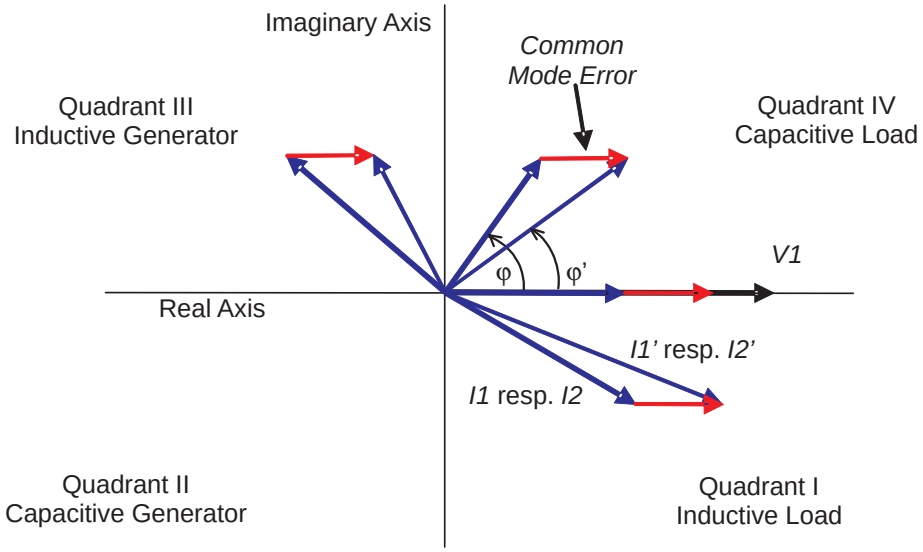
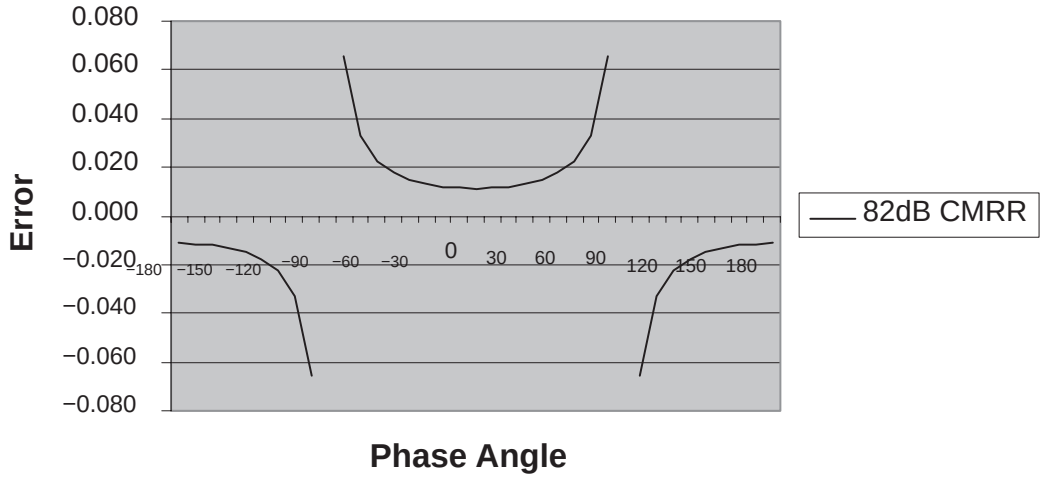


Figure 1−5 shows the dependence of the measurement error to the phase angle φ. It is described by the $\cos^{-1}\varphi$ function.

Figure 1−5. E-Meter Error Due to CMRR



Due to the constant value and phase angle of the introduced common mode error, it is possible to correct this error: it is only necessary to subtract its value from all measured active energy values.

The value in address CMRRCOMP controls the common mode rejection function of the ESP430CE1A:

- If (CMRRCOMP) = 0: the common mode rejection function is switched off.
- If (CMRRCOMP) > 0: the value is a quarter of the actual value to be used. This is to allow also the compensation of small common mode influences.

The value in CMRRCOMP is approximately given by:

$$(\text{CMRRCOMP}) = 0.25 \times 10^{(0.05 \times \text{CMRR})}$$

The compensation value (CMRRCOMPStore) for the active energies is calculated with the formula:

$$(\text{CMRRCOMPStore}) = \frac{(\text{V1RMS})^2}{4 \times (\text{CMRRCOMP})}$$

(CMRRCOMPStore) is used for the correction of all measured active energies:

- Active energy for 4096 samples (ACTENERGY1 and ACTENERGY2). The common mode correction is made with the value for (CMRRCOMPStore) of the actual 4096 samples.
- Active energy for a single mains period (ACTENSPER1 and ACTENSPER2). The common mode correction is made with the value for (CMRRCOMPStore) of the last 4096 samples, not of the actual ones: the actual value of (CMRRCOMPStore) is not yet available.
- Active energy used with bit ILREACHEDFG if bit MB = 0 (ILREACHEDFG is set dependent on the reached energy level). The common mode correction is made with the value for (CMRRCOMPStore) of the last 4096 samples, not of the actual ones: the actual value for (CMRRCOMPStore) is not yet available.

The reactive energy is not influenced by the common mode and, therefore, needs no correction.

The apparent energy is calculated with the corrected active energy and the not influenced reactive energy, and is also correct.

1.2.11 Maximum Spike for V_1 Filter (ESP430CE1A Only)

The value in DELTAV1MAX defines the maximum tolerable change from one V1 sample to the next one if the V1 Filter is enabled (bit V1FILTER = 1). If the V1 Filter is enabled and the change from one V1 sample to the last one exceeds the value in DELTAV1MAX (absolute values are used) then a linear approximation is made for the value N_{v1n}. Otherwise the N_{v1n} value is used unmodified.

Format	Unsigned Integer Word	+16.0
Range	0x00 to 0x0FFFF	0.0 to +65,535
Resolution	1 step	
Initialization	0x0	

Formulas:

$$|N_{v1n} - N_{v1n-1}| < (\text{DELTAV1MAX}) \rightarrow \text{sample v1n is used as is}$$

$$|N_{v1n} - N_{v1n-1}| \geq (\text{DELTAV1MAX}) \rightarrow N_{v1n} = (N_{v1n-1} - N_{v1n-2}) + N_{v1n-1} = 2N_{v1n-1} - 2N_{v1n-2}$$

$$(\text{DELTAV1MAX}) \geq 2\pi \times f_{\text{mains max}} \times \frac{N_{\text{ADC max}}}{f_{\text{ADC}}} \times k_{\text{safety}} \quad \text{value for(DELTAV1MAX)}$$

Example: The V1FILTER is used with a used ADC range of 95 %, a maximum mains frequency of 66 Hz, an ADC frequency of 2048 Hz and a safety factor 1.2. The value for (DELTAV1MAX) is:

$$(\text{DELTAV1MAX}) \geq 2\pi \times 66 \times \frac{0.95 \times 0\text{x7FFF}}{2048} \times 1.2 = 7564 = 0\text{x1D8B}$$

1.2.12 Common Mode Rejection Ratio (ESP430CE1A Only)

The value in CMRRCOMP defines the value of the common mode rejection ratio for the two current ADCs due to the voltage ADC. If the value in CMRRCOMP is zero, no correction of the common mode influence is made. The value in CMRRCOMP is multiplied by 4 before its use to allow also the compensation of small common mode influences. The calculated compensation value is stored in the RAM address CMRRCOMPStore and used for the correction of all active energies (4096 samples, single mains period and energy level count (bit MB = 0)). The correction depends on the squared value of (V1RMS).

Format	Unsigned Integer Word	+16.0
Range	0x00 to 0x0FFFF	0.0 to +262,140 (108.37 dB)
Resolution	4	
Initialization	0x0	

Formulas:

$$(\text{CMRRCOMPStore}) = \frac{(\text{V1RMS})^2}{4 \times (\text{CMRRCOMP})} \ [\text{steps}^2]$$

$$(\text{CMRRCOMPStore}) = \frac{(\text{V1RMS})^2}{4 \times (\text{CMRRCOMPStore})} \ [1]$$

Example: The necessary CMRR compensation for active energy 1 is 3554 steps^2 . The measured RMS value V1RMS for voltage V_1 is 29EAh. This leads to a value for CMRRCOMP:

$$(\text{CMRRCOMPStore}) = \frac{(\text{V1RMS})^2}{4 \times (\text{CMRRCOMPStore})} = \frac{0\text{x29EA}^2}{4 \times 3554} = 8098.82$$

The rounded value 8099 (1FA3h) is written to address CMRRCOMP.

Example: an electricity meter showed the following common mode errors for small currents dependent on the phase angle ? (the absolute value of all four |cosφ| = 0.5):

I_1 = 10 A (10% I_{max}), φ = 0 º, Err_{Hi} = +0.1 % calibrated value
I_1 = 0.2 A (0.2% I_{max}), φ = +120º, Err_{Lo120} = −1.8%
I_1 = 0.2 A (0.2% I_{max}), φ = +60º, Err_{Lo60} = +2.2%
I_1 = 0.2 A (0.2% I_{max}), φ = 0º, Err_{Lo0} = +1.4%
I_1 = 0.2 A (0.2% I_{max}), φ = −60º, Err_{Lo-60} = +1.9%
I_1 = 0.2 A (0.2% I_{max}), φ = −120º, Err_{Lo-120} = −2.2%

The measured RMS value (V1RMS) for voltage V_1 is 29EAh.

The correct value for (ACTENERGY1) for I_1 = 0.2 A and φ = 0º is 5,33E1h.

The necessary correction value for the active energies (CMRRCOMPStore) gets:

$$(\text{CMRRCOMPStore}) = 0.25 \times (|\text{Err}_{\text{Lo120}}| + |\text{Err}_{\text{Lo60}}| + |\text{Err}_{\text{Lo}-60}| + |\text{Err}_{\text{Lo}-120}|) \times (\text{ACTENERGY1}) \times |\cos\phi|$$

$$(\text{CMRRCOMPStore}) = 0.25 \times (|-0.018| + |0.022| + |0.019| + |-0.022|) \times 533\text{E1h} \times 0.5 = 3452.23$$

To get the needed correction value 3452 with the measured V_1 voltage:

$$(\text{CMRRCOMPStore}) = \frac{(\text{V1RMS})^2}{4 \times (\text{CMRRCOMPStore})} = \frac{0\text{x29EA}^2}{4 \times 3452.23} = 8337.57$$

The rounded value 8338 is written to address CMRRCOMP. The correction value (CMRRCOMPStore) gets:

$$(\text{CMRRCOMPStore}) = \frac{(\text{V1RMS})^2}{4 \times (\text{CMRRCOMP})} = \frac{0\text{x29EA}^2}{4 \times 8338} = 3452.05$$

With this correction value, the six measured errors improve to:

I_1 = 10 A (10% I_{max}), φ = 0 º, Err_{Hi} = −202 ppm calibrated value
I_1 = 0.2 A (0.2% I_{max}), φ = +120º, Err_{Lo120} = +0.22%
I_1 = 0.2 A (0.2% I_{max}), φ = +60º, Err_{Lo60} = +0.17%
I_1 = 0.2 A (0.2% I_{max}), φ = 0º, Err_{Lo0} = +0.39%
I_1 = 0.2 A (0.2% I_{max}), φ = −60º, Err_{Lo-60} = −0.12%
I_1 = 0.2 A (0.2% I_{max}), φ = −120º, Err_{Lo-120} = −0.18%

NOTE: If the phase angles used for the calculation above show different values for |cos φ|, then a correction to equal absolute phase angles is necessary. This is made with the formula:

$$Err_{Lo\phi corr} = Err_{Lo\phi} \times \frac{\cos\phi}{\cos\phi_{corr}}$$

For example, the 120º error Err_{Lo120} is measured with a phase angle φ = +124º, due to the calibration equipment.

I_1 = 0.2 A (0.2% I_{max}), φ = +124º, Err_{Lo124} = −2.0%

$$Err_{Lo120} = Err_{Lo124} \times \frac{\cos\phi}{\cos\phi_{corr}} = -2.0\% \times \frac{\cos 124}{\cos 120} = -2.237\%$$

The corrected electricity meter error with φ = +120º is −2.237%.

1.2.13 ESP430CE1(A) Return Register Description

The Return registers are used to pass calculated results and status information from the ESP430 to the CPU.

ESP430_STAT0: Embedded Processor Status Register 0

ESP430_STAT0 and the ESP430_STAT1 indicate the occurrence of ESP430CE1(A) events to the CPU. The ESP430_STAT1 is present only in the ESP430CE1A. When the corresponding enable bit is set in the EVENT parameter register, a change in value from 0 to 1 of each ESP430_STAT0/ESP430_STAT1 bit triggers a mailbox message to be sent from the ESP430 to the CPU. ESP430_STAT0 and ESP430_STAT1 flags are set independently of the settings in EVENT and are described in Table 1?10 and Table 1−11, respectively.

Table 1−10. ESP430_STAT0 Bit Summary

Name	Bit Function
ACTIVEFG	Indicates the ESP430 is in MEASURE or CALIBRATION mode and is active.
I2PEAKFG	Indicates an overcurrent condition has occurred on I_2 as defined by IPEAKLEVEL when exceeded for three contiguous I_2 samples. When set, the larger I_x value is stored in IPEAK. Cannot be cleared by the CPU.
I1PEAKFG	Indicates an overcurrent condition has occurred on I_1 as defined by IPEAKLEVEL when exceeded for three contiguous I_1 samples. When set, the larger I_x value is stored in IPEAK. Cannot be cleared by the CPU.
VPEAKFG	Indicates an overvoltage condition has occurred on V_1 as defined by VPEAKLEVEL when exceeded for three contiguous V_1 samples. Cannot be cleared by the CPU.
VDROPFG	Indicates and undervoltage condition has occurred on V_1 as defined by VDROPLEVEL and VDROPCYCLS. Cannot be cleared by the CPU.
NEGENFG	Indicates that negative energy has been accumulated over the last 4096 measurements. This can be caused by meter tampering or delivery of energy into the line by the load. Treatment of negative energy is defined by ESP430_CTRL0 bits NE0 and NE1. Cannot be cleared by the CPU.

Table 1−10. ESP430_STAT0 Bit Summary (continued)

Name	Bit Function
TAMPFG	Indicates possible meter tampering has occurred. See ESP430CE1 Energy Measurement Configurations for more information on tamper detection. Cannot be cleared by the CPU.
CALRDYFG	Indicates the end of the calibration routine and availability of new active energy values in ACTENERGYx. This flag only applies when the ESP430 is in CALIBRATION mode. Cleared when the ESP430 is sent into IDLE mode.
ZXTRFG	Indicates the occurrence of a trailing-edge zero crossing (positive-to-negative) on V_1. The following tasks are performed following a trailing-edge zero crossing: − If pending, a temperature measurement is initiated − Undervoltage checks are performed for the last mains period and VDROPFG is set accordingly. All tasks except the temperature result are completed with the next available waveform samples after the zero crossing indicated by WFSRDYFG immediately after ZXTRFG has been set. To simplify flag handling ZXLDFG can be used to indicate completion of the ZXTRFG tasks. Cleared when a leading-edge zero crossing occurs and cannot be reset by the CPU.
ZXLDFG	Indicates the occurrence of a leading-edge zero crossing (negative-to-positive) on V_1. The following tasks are performed following a leading-edge zero crossing: − If pending, a temperature measurement is initiated − MAINSPERIOD is calculated and updated − Load type is determined and an internal counter increments for a capacitive load or decrements for an inductive load. This value is written to CAPIND after every 4096 mains periods. − LINECYCLCNT increments − ACTENSPER1 and ACTENSPER2 are are updated − VPEAK and IPEAK are updated All tasks except the temperature result are completed with the next available waveform samples after the zero crossing indicated by WFSRDYFG immediately after ZXLDFG has been set. To simplify flag handling ZXTRFG can be used to indicate completion of the ZXLDFG tasks. Cleared when a trailing-edge zero crossing occurs and cannot be reset by the CPU.
ENRDYFG	Indicates new calculated ESP430 values are ready. Associated registers are V1RMS, IRMS, ACTENERGYx, REACTENERGY, APPENERGY, POWERFCT and CAPIND. Cleared when the event message is sent or by the mCLR_EVENT control command.
ILREA-CHEDFG	Indicates that the interrupt level threshold for energy accumulation or number of measurements performed was reached as defined by the INTRPTLEVL parameter register and the MB control bit in ESP430_CTRL0. Cleared when the event message is sent or by the mCLR_EVENT control command.
I2GTI1FG	Indicates the current channel with the larger RMS value over the last 4096 samples and is set when I_2 RMS > I_1 RMS if CURR_I2 = 1. I2GTI1FG is always zero when CURR_I2 = 0. Cannot be cleared by the CPU.
WFSRDYFG	Indicates new waveform samples are ready in WAVEFSV1, WAVEFSI1 and WAVEFSI2 registers. Cleared when the event message is sent or by the mCLR_EVENT control command.

Table 1−11. ESP430_STAT1 Bit Summary†

Name	Bit Function
Reserved	Bits 0 and 1 are reserved.
ILNEGFG	Interrupt Level Negative Bit. The ILNEGFG Bit (bit 2) indicates the sign of the energy of the reached Interrupt Level.
	ILNEGFG = 0: energy is positive
	ILNEGFG = 1:energy is negative
	Set if the energy of the reached interrupt level is negative. Reset if the energy of the reached interrupt level is positive. It is not reset by sending an event message or with the command CLR_EVENT.
Reserved	Bits 3 to 9 are reserved.
V1PEAKNEGFG	V_1 Negative Peak Bit. The V1PEAKNEGFG Bit (bit 10) indicates the sign of the measured V_1 peak.
	V1PEAKNEGFG = 0: Last V_1 peak was positive
	V1PEAKNEGFG = 1: Last V_1 peak was negative
	The bit is not reset by sending an event message or with the command CLR_EVENT.
I1PEAKNEGFG	I_1 Negative Peak Bit. The I1PEAKNEGFG Bit (bit 11) indicates the sign of the measured I_1 peak.
	I1PEAKNEGFG = 0: Last I_1 peak was positive
	I1PEAKNEGFG = 1: Last I_1 peak was negative
	The bit is not reset by sending an event message or with the command CLR_EVENT.
I2PEAKNEGFG	I_2 Negative Peak Bit. The I2PEAKNEGFG Bit (bit 12) indicates the sign of the measured I_2 peak.
	I2PEAKNEGFG = 0: Last I_2 peak was positive
	I2PEAKNEGFG = 1: Last I_2 peak was negative
	The bit is not reset by sending an event message or with the command CLR_EVENT.
Reserved	Bits 13 to 15 are reserved.

† Present only in the ESP430CE1A

WAVEFSV1: V_1 Waveform Sample

The last offset-corrected ADC sample for V_1 is in WAVEFSV1. The correction of the original ADC result N_{V1ADC} is made with the offset correction for V_1 contained in V1OFFSET and a 2nd offset depending on bit DCREM_V1.

Format	Signed Integer	±15.0
Range	0x8000 to 0x07FFF	−32768 to +32767
Resolution	1 step	

Formulas:

DCREM_V1 = 0:

$$(\text{WAVEFSV1}) = N_{V1ADC} - N_{V1SC} + (\text{V1OFFSET})$$

DCREM_V1 = 1:

$$(\text{WAVEFSV1}) = N_{V1} = N_{V1ADC} - N_{V1DCREM} + (\text{V1OFFSET})$$

$$V_1 = k_{V1} \times (\text{WAVEFSV1})$$

Where:

N_{V1ADC}: Conversion value from SD16 V_1 channel

N_{V1SC}: ESP430-corrected offset value taken during INIT with shunted SD16 V_1 channel inputs.

$N_{V1DCREM}$: ESP430-corrected offset value calculated by the DC removal algorithm (see DCREM_V1 description)

V_1: Meter-specific result obtained by multiplying WAVEFSV1 with the meter constant k_{V1}.

Example: An input voltage sample corresponding to a conversion result of 0x32D8 was measured. DCREM_V1 = 0 (DC removal function is off). The value for N_{V1SC} = 0xFFFB (−0x5) and V1OFFSET = 0x13. WAVEFSV1 is calculated as:

$$(\text{WAVEFSV1}) = 0x32D8 + 0x5 + 0x13 = 0x32F0$$

WAVEFSIx: I_X Waveform Sample

The last offset-corrected ADC sample for I_X is in WAVEFSIx, where x = 1 or 2 for I_1 or I_2, respectively. The correction of the original ADC result N_{IxADC} is made with the offset correction for I_X contained in IxOFFSET, a 2nd offset depending on bit DCREM_Ix and the adaptation value for I_X in ADAPTIx.

Format	Signed Integer	±15.0
Range	0x8000 to 0x07FFF	−32768 to +32767
Resolution	1 step	

Formulas:

DCREM_Ix = 0:

$$(\text{WAVEFSIx}) = (N_{IXADC} - N_{IXSC} + (\text{IxOFFSET})) \times (\text{ADAPTIx}) \times 2^{-14}$$

DCREM_Ix = 1:

$$(\text{WAVEFSIx}) = (N_{IxADC} - N_{IxDCREM} + (\text{IxOFFSET})) \times (\text{ADAPTIx}) \times 2^{-14}$$

$$I_x = k_{Ix} \times (\text{WAVEFSIx})$$

Where:

N_{IxADC}: Conversion value from SD16 Ix channel

N_{IxSC}: ESP430-corrected offset value taken during INIT with shunted SD16 I_X channel inputs.

$N_{IxDCREM}$: ESP430-corrected offset value calculated by the DC removal algorithm (see DCREM_Ix description)

I_X: Meter-specific result obtained by multiplying WAVEFSIx with the meter constant k_{IX}.

Example: An input current sample corresponding to a conversion result of 0x1234 on I1 was measured. DCREM_I1 = 1 (DC removal function is on), the value for $N_{I1DCREM}$ = 0xFFFB (−0x5) and I1OFFSET = 0xFFEF (−0x11). With ADAPTI1 = 0x40CF (1.01264) the corrected value written to WAVEFSI1 is:

$$(\text{WAVEFSI1}) = (0x1234 - 0xFFFB + 0xFFEF) \times 0x40CF \times 2^{-14} = 0x1262$$

ACTENERGYx: I_X Active Energy

The calculated active energy of I_X for the last 4096 ADC measurements is stored in ACTENERGYx, where x = 1 or 2 for I_1 and I_2, respectively. This value also represents the average active power P_{actx} over the same measurement time (ACTENERGYx = ACTENERGYx_HI, ACTENERGYx_LO = 32 bits).

ESP430CE1A Only

The comparison of the two absolute, active energies (ACTENERGY1) and (ACTENERGY2) defines the flag I2GTI1FG (I_2 greater than I_1):

- ❏ If |(ACTENERGY1)| ≥ |(ACTENERGY2)|: I2GTI1FG = 0
- ❏ If |(ACTENERGY2)| > |(ACTENERGY1)|: I2GTI1FG = 1

The compensation value (CMRRCOMPStore) for the common mode influence is subtracted from the calculated active energy 1. The compensation value is zero if the common mode compensation is switched off ((CMRRCOMP) = 0).

ESP430CE1A Only

The comparison of the two absolute, active energies (ACTENERGY1) and (ACTENERGY2) defines the flag I2GTI1FG:

- ❏ If |(ACTENERGY1)| ≥ |(ACTENERGY2)|: I2GTI1FG = 0
- ❏ If |(ACTENERGY2)| > |(ACTENERGY1)|: I2GTI1FG = 1

The compensation value (CMRRCOMPStore) for the common mode influence is subtracted from the calculated active energy 2 if bit I2CMRR = 1 in ESP430_CTRL0. The compensation value is zero if the common mode compensation is switched off ((CMRRCOMP) = 0).

Format	Signed integer	±31.0
Range	0x8000,0000 to 0x07FFF,FFFF	
Resolution	1 step^2 = 1/C_{Z1}	Normal Operation
	16 steps^2 = 16/C_{Zx}	Calibration Mode

Formulas:

$$(\text{ACTENERGYx}) = \frac{1}{4096} x \sum_{i=1}^{4096} (\text{WAVEFSV1}) x (\text{WAVEFSIx}) \; [\text{steps}^2]$$

Energy:

$$W_{actx} = \frac{(\text{ACTENERGYx})}{C_{Zx}} = (\text{ACTENERGYx}) \times k_{Ix} \times k_{V1} \times \frac{4096}{f_{ADC}} \; [\text{Ws}]$$

Power:

$$P_{actx} = \frac{(\text{ACTENERGYx})}{C_{Zx}} \; x \; \frac{f_{ADC}}{4096} = (\text{ACTENERGYx}) \times k_{Ix} \times k_{V1} \; [\text{W}]$$

Note: ACTENERGYx and STARTCURR

When the RMS value for I_X is smaller than the value in STARTCURR, ACTENERGYx is set to zero.

REACTENERGY: Reactive Energy

The calculated reactive energy of the last 4096 measurements is stored in REACTENERGY. This value also represents the average reactive power P_{react} over the same measurement time.

(REACTENERGY = REACTENERGY_HI, REACTENERGY_LO = 32 bits)

I2GTI1FG determines if the reactive energy is calculated for I_1 or I_2. The larger current is always used for the calculation of REACTENERGY.

- ❏ I2GTI1FG = 0: ACTENERGY1 and APPENERGY are used to calculate W_{react}
- ❏ I2GTI1FG = 1: ACTENERGY2 and APPENERGY are used to calculate W_{react}

ESP430CE1

Format	Unsigned integer	+31.0
Range	0x0000,0000 to 0x07FFF,FFFF	
Resolution	1 step^2 = 1/C_Z = 1/C_{Z1} = 1/C_{Z2}	

ESP430CE1A

Format	Signed integer	±31.0
Range	0x8000,0000 to 0x07FFF,FFFF	
Resolution	1 step^2 = 1/C_Z = 1/C_{Z1} = 1/C_{Z2}	

Formulas:

I2GTI1FG = 0:

$$(\text{REACTENERGY}) = \sqrt{(\text{APPENERGY})^2 - (\text{ACTENERGY1})^2}\ [\text{steps}^2]$$

$$W_{react} = \frac{(\text{REACTENERGY})}{C_{Z1}} = (\text{REACTENERGY}) \times k_{I1} \times k_{V1} \times \frac{4096}{f_{ADC}}\ [\text{Ws}]$$

I2GTI1FG = 1:

$$(\text{REACTENERGY}) = \sqrt{(\text{APPENERGY})^2 - (\text{ACTENERGY2})^2}\ [\text{steps}^2]$$

$$W_{react} = \frac{(\text{REACTENERGY})}{C_{Z2}} = (\text{REACTENERGY}) \times k_{I2} \times k_{V1} \times \frac{4096}{f_{ADC}}\ [\text{Ws}]$$

The average reactive power of the last 4096 measurements is:

I2GTI1FG = 0:

$$P_{react} = \frac{(\text{REACTENERGY})}{C_{Z1}} \times \frac{f_{ADC}}{4096} = (\text{REACTENERGY}) \times k_{I1} \times k_{V1}\ [\text{W}]$$

I2GTI1FG = 1:

$$P_{react} = \frac{(\text{REACTENERGY})}{C_{Z2}} \times \frac{f_{ADC}}{4096} = (\text{REACTENERGY}) \times k_{I2} \times k_{V2}\ [\text{W}]$$

APPENERGY: Apparent Energy

The calculated apparent energy of the last 4096 measurements is stored in APPENERGY. This value also represents the average apparent power P_{app} over the same measurement time.
(APPENERGY = APPENERGY_HI, APPENERGY_LO = 32 bits)

I2GTI1FG determines if the apparent energy is calculated for I_1 or I_2. The larger current is always used for the calculation of APPENERGY.

- ❏ I2GTI1FG = 0: I_1 RMS = IRMS and V1RMS are used for the calculation
- ❏ I2GTI1FG = 1: I_2 RMS = IRMS and V1RMS are used for the calculation

Format	Signed integer	±31.0
Range	0x8000,0000 to 0x07FFF,FFFF	
Resolution	1 step^2 = 1/C_Z = 1/C_{Z1} = 1/C_{Z2}	

Formulas:
Apparent energy:

$$(\text{APPENERGY}) = (\text{V1RMS})\text{x}(\text{IRMS})\ [\text{steps}^2]$$

I2GTI1FG = 0:

$$W_{app} = \frac{(\text{APPENERGY})}{C_{Z1}} = (\text{APPENERGY}) \times k_{I1} \times k_{V1} \times \frac{4096}{f_{ADC}}\ [\text{Ws}]$$

I2GTI1FG = 1:

$$W_{app} = \frac{(\text{APPENERGY})}{C_{Z2}} = (\text{APPENERGY}) \times k_{I2} \times k_{V1} \times \frac{4096}{f_{ADC}}\ [\text{Ws}]$$

Average apparent power:
I2GTI1FG = 0:

$$P_{app} = \frac{(\text{APPNERGY})}{C_{Z1}} \times \frac{f_{ADC}}{4096} = (\text{APPENERGY}) \times k_{I1} \times k_{V1}\ [\text{W}]$$

I2GTI1FG = 1:

$$P_{app} = \frac{(\text{APPNERGY})}{C_{Z2}} \times \frac{f_{ADC}}{4096} = (\text{APPENERGY}) \times k_{I2} \times k_{V2}\ [\text{W}]$$

ACTENSPERx: I_X Active Energy over a Single Mains Period

The calculated active energy of I_X during the last mains period is stored in ACTENSPERx, where x = 1 or 2 for I_1 or I_2, respectively. ACTENSPERx is calculated with each leading edge zero crossing of the mains voltage and is useful for calibration purposes. The availability of the latest calculated result is indicated by WFSRDYFG after ZXLDFG = 1.
(ACTENSPERx = ACTENSPERx_HI, ACTENSPERx_LO = 32 bits)

ESP430CE1A Only

The compensation value (CMRRCOMPStore) for the common mode influence is corrected with the measured mains period at address MAINSPERIOD and subtracted from the calculated active energy 1. The compensation value is zero if the common mode compensation is switched off ((CMRRCOMP) = 0). For (CMRRCOMPStore) the value of the last 4096 samples is used: the new value is not yet available.

Format	Signed integer	±31.0
Range	0x8000,0000 to 0x07FFF,FFFF	
Resolution	1 step^2 = 1/C_{Zx}	

Formulas:

Energy during last mains period:

$$W_{xSP} = \frac{(ACTENSPERx)}{C_{Zx}} \text{ [Ws]}$$

Power during last mains period:

$$P_x = \frac{(ACTENSPERx)}{C_{Zx} \times T_{mains}} = (ACTENSPERx) \times k_{Ix} \times k_{V1} \times \frac{4096}{f_{ADC}} \times f_{MAINS} =$$

$$= (ACTENSPER1) \times k_{Ix} \times k_{V1} \times \frac{4096 \times 256}{(MAINSPERIOD)} \text{ [W]}$$

Jitter of the energy value in ACTENSPERx is small when voltage and current have constant values and is due to the small uncertainty of the measured energy near the zero crossing of the voltage. The jitter *e* coming from this uncertainty for PF = 1 is:

$$e = \frac{\pm \left(\sin\left(\frac{f_{mains}}{f_{ADC}} \times 360^o\right)\right)^2}{\frac{f_{ADC}}{f_{mains}} \times 2}$$

For f_{mains} = 50 Hz and f_{ADC} = 4096 Hz the resulting jitter e (relative to 1.0) is:

$$e = \pm \frac{\left(\sin\left(\frac{50}{4096} \times 360^o\right)\right)^2}{\frac{4096}{50} \times 2} = \pm \frac{(\sin 4.39453)^2}{81.92 \times 2} = \pm\ 143.34Ex10^{-6}$$

Note: Treatment of Negative Energy

When negative active energy is measured, ACTENSPERx is not set to zero. The measured energy is always calculated and provided in the appropriate return register.

POWERFCT: Power Factor

The calculated power factor of the last 4096 measurements is stored in POWERFCT. I2GTI1FG determines if the power factor is calculated for I_1 or I_2. The larger current channel is always used for the calculation.

- ❏ I2GTI1FG = 0: ACTENERGY1 and APPENERGY are used for the calculation
- ❏ I2GTI1FG = 1: ACTENERGY2 and APPENERGY are used for the calculation

Format	Unsigned Integer.Fraction	+1.14
Range	0x00 to 0x4000	0.0 to 1.000
Resolution	61.035×10^{-6}	2^{-14}

Formulas:

$$(\text{POWERFCT}) = \frac{(\text{ACTENERGYx})}{(\text{APPENERGY})}$$

$$\text{PF} = (\text{POWERFCT}) \times 2^{-14}$$

Example: POWERFCT contains the calculated value 0x2ABC. The corresponding power factor PF is:

$$\text{PF} = 0\text{x2ABC} \times 2^{-14} = 0.66772$$

For a pure sinusoid, PF = cosφ. This results in:

$$\varphi = \arccos(\text{PF}) = \arccos(0.66772) = 48.108^{\circ}$$

Note: The sign of the angle is indicated by the value in CAPIND.

Note: Power Factor Angle

The sign of the calculated angle is indicated by the value in CAPIND.

Note: ESP430CE1A Only

The nature of the angle φ (inductive or capacitive load) can be seen in (REACTENERGY). The reactive energy is negative for capacitive loads and positive for inductive loads.

CAPIND: Capacitive/Inductive Indication

The average phase shift during the last 4096 measurements is stored in CAPIND. With each leading-edge zero crossing of V_1, the phase shift between the selected current I_x and V_1 is calculated where x = 1 or 2 for I_1 or I_2, respectively. I2GTI1FG determines if CAPIND is calculated for I_1 or I_2. The larger current of the last 4096 measurements is always used for the calculation.

If the current lags the voltage (inductive phase shift) an internal counter decrements. If the current leads the voltage (capacitive phase shift), the counter increments. For a zero phase shift the counter is not changed. The internal counter value is written to CAPIND after 4096 measurements and reset.

Format	Signed word	±15.0
Range	0x8000 to 0x7FFF	−32,768 to +32,767
Resolution	1 mains cycle	

Formulas:

$$\text{If (CAPIND)} > 0 : \text{capacitive phase shift}$$

$$\text{If (CAPIND)} = 0 : \text{no phase shift}$$

$$\text{If (CAPIND)} < 0 : \text{inductive phase shift}$$

Example: CAPIND contains the value 0xFFFE (−0x2). This indicates a small average inductive phase shift during the last 4096 measurements. This is normally caused by power factors close to 1.0. The corresponding power factor is contained in POWERFCT.

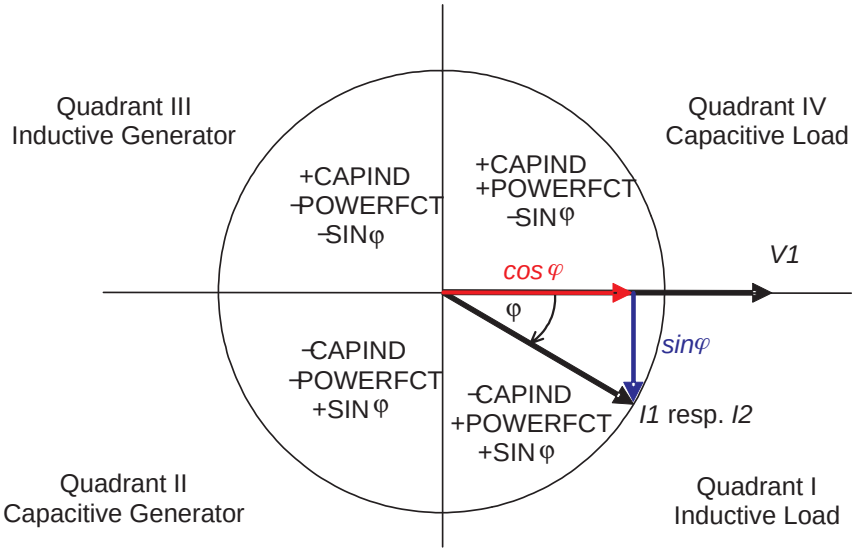
Inductive/Capacitive Indication

Energy measurement for the full 360° range of φ is possible with NEx = 10b (see Table 1−12).

Table 1−12. Four Quadrant Energy Measurement IEC 62053−23

CAPIND	POWERFCT	Sin	Quadrant	Energy	Reactive Energy†
Negative	Positive	Positive	I	Inductive load	Positive
Negative	Negative	Positive	II	Capacitive generator	Positive
Positive	Negative	Negative	III	Inductive generator	Negative
Positive	Positive	Negative	IV	Capacitive load	Negative

† The sign of sinφ shows the sign of the involved reactive power.
ESP430CE1: The reactive power (REACTENERGY) is an absolute value (always positive).
ESP430CE1A: The reactive power (REACTENERGY) is a signed value with the sign of sinφ.
IEC 62053−23: The phase angle between current I_1 or I_2 and voltage V1 is defined to be positive in the clockwise direction.



ESP430CE1A Only

The average phase sequence during the last 4096 measurements is stored in word CAPIND: with each leading zero crossing of the mains voltage, the phase shift between the selected current Ix and voltage V1 is calculated. The flag I2GTI1FG decides if CAPIND is calculated for current I1 or current I2. This means the higher current of the last 4096 measurements is used for the calculation.

- ❏ I2GTI1FG = 0: I1 is used for the calculation
- ❏ I2GTI1FG = 1: I2 is used for the calculation

If the current lags the voltage (inductive phase shift) an internal counter is decremented, if the current leads the voltage (capacitive phase shift), the counter is incremented. If the phase shift is zero, the counter is not changed.

The check for leading or lagging of the current is made with each leading zero voltage crossing of voltage V1.

The counter is written to word CAPIND after 4096 measurements and then cleared.

Flags NE0 and NE1 indicate the update of (CAPIND).

Format	Signed integer	+15.0
Range	$\pm f_{mains} \times 4096/f_{ADC}$	−264 to +264 (f_{mains} = 66 Hz, f_{ADC} = 1024 Hz)
Resolution	1 mains cycle	

Formulas:

If (CAPIND) > 0: Capacitive phase shift

If (CAPIND) = 0: No phase shift (resistive)

If (CAPIND) < 0: Inductive phase shift

Example: (CAPIND) contains the value 0xFFFE (−2). This indicates a small average inductive phase shift during the last second. This is normally caused by power factors cosφ very near to 1.0. The corresponding cosφ is contained in word POWERFCT.

MAINSPERIOD: Calculated Mains Period

The mains period T_{mains} is calculated and stored in MAINSPERIOD. The value for MAINSPERIOD is measured between two leading-edge zero crossings of V_1 and is updated for each mains period.

Format	Unsigned integer	+15.0
Range	0x00 to 0x7FFF	0 to +32767
Resolution	1 ESP430 time base unit	

Formulas:

$$T_{mains} = (\text{MAINSPERIOD}) \times \frac{1}{f_{ADC} \times 256} \text{ [s]}$$

Example: MAINSPERIOD contains the value 0x5050 where f_{ADC} = 4096 Hz (1 ESP430 time base unit = 2^{-20} s = 954 ns). The corresponding mains period T_{mains} is:

$$T_{mains} = 0x5050 \times 2^{-20} = 19.607 \text{ [ms]}$$

This equals a mains frequency of approximately 51Hz.

V1RMS: V_1 RMS Voltage

The value in V1RMS represents the calculated RMS value of V_1 for the last 4096 voltage samples. The offset corrected ADC samples given in WAVEFSV1 are used for the calculation.

Format	Unsigned integer	+15.0
Range	0x00 to 0x7FFF	0 to +32767
Resolution	1 step = 1 k_{V1}	

Formulas:

$$(\text{V1RMS}) = \sqrt{\frac{1}{4096} x \sum_{i=1}^{4096} (\text{WAVEFSV1})^2} \text{ [steps]}$$

$$v1_{RMS} = k_{V1} \times (\text{V1RMS}) \text{ [V]}$$

Example: V1RMS contains the value 0x3BCC (15,308). With $k_{V1} = 15.365513x10^{-3}$, this corresponds to an RMS value for V_1 of:

$$v1_{RMS} = 15.365513x10^{-3} \times 0x3BCC = 235.22 \text{ [V]}$$

IRMS: I_1 or I_2 RMS Current

The value in IRMS represents the RMS value of the current I_1 or I_2 for the last 4096 measurements. The corrected ADC samples in WAVEFSI1 or WAVEFSI2 are used for the calculation. If two current sensors are used, I_1 RMS and I_2 RMS are internally calculated and compared. I2GTI1FG is set according to the result and the larger value is given in IRMS.
(IRMS = IRMS_HI.IRMS_LO = 32 bits)

- I_1 RMS $\geq I_2$ RMS: I2GTI1FG = 0, I_1 RMS is stored in IRMS
- I_1 RMS $< I_2$ RMS: I2GTI1FG = 1, I_2 RMS is stored in IRMS

Format	Unsigned Integer.Fraction	+15.2
Range	0x0.0 to 0x07FFF.C000	0.0 to +32,767.75
Resolution	0.25 steps = 0.25 k_{Ix}	

Formulas:

I2GTI1FG = 0:

$$(\text{IRMS}) = \sqrt{\frac{1}{4096} x \sum_{i=1}^{4096} (\text{WAVEFSI1})^2} \text{ [steps]}$$

$$i1_{RMS} = k_{I1} \times (\text{IRMS}) \text{ [A]}$$

I2GTI1FG = 1:

$$(\text{IRMS}) = \sqrt{\frac{1}{4096} x \sum_{i=1}^{4096} (\text{WAVEFSI2})^2} \text{ [steps]}$$

$$i2_{RMS} = k_{I2} \times (\text{IRMS}) \text{ [A]}$$

Example: IRMS contains the value 0x5A1C.4 (23,068.25). For $k_{I1} = 2.21946x10^{-3}$, this corresponds to an RMS value for I_1 of:

$$i1_{RMS} = 2.21946x10^{-3} \times 0x5A1C.4 = 51.2 \text{ [A]}$$

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Voltage V_1 is in range:

The values of the apparent energy (APPENERGY) and the RMS value of voltage V_1 (V1RMS) are used for the calculation of I1RMS, without regard to I2RMS. If two current sensors are in use, the flag I2GTI1FG defines for which current the RMS value is calculated:

- If I2GTI1FG = 0 (I1RMS) is stored in (IRMS)
- If I2GTI1FG = 1 (I2RMS) is stored in (IRMS)

For a better resolution the 16 bits of the fractional part are stored, too. The (IRMS) value is used for the start current detection.

Flags NE0 and NE1 indicate the update of (IRMS).

Format	Unsigned Integer.Fraction	+15.16 in two words
Range	0x0.0 to 0x07FFF.FFFF	0.0 to +32,767.99
Resolution	2^{-16} steps	

Formulas:

$$I_{sRMS} = \sqrt{\frac{\sum_{n=0}^{4095} i_{sn}^{2}}{4096}} \text{ [A]} \qquad \text{Definition}$$

$$(IRMS) = \frac{(APPENERGY)}{(V1RMS)} \text{ [steps]} \qquad I_{sRMS} = (IRMS) \times K_{Is} \text{ [A]}$$

$$I_{sRMS} = \frac{I_{spp}}{2} \times \sqrt{0.5} \text{ [A]} \qquad \text{For sinusoidal currents}$$

When voltage V1 is very low or missing:

The summed, absolute values of I_1 and I_2 (representing the mean values of I_1 and I_2) are used for the calculation of I1RMS and I2RMS. If two current sensors are in use, the flag I2GTI1FG is defined by the two summed−up values of (I1mean) and (I2mean):

- If (I1mean) ≥ (I2mean): I2GTI1FG = 0 (I1mean) is used for the calculation
- If (I1mean) < (I2mean): I2GTI1FG = 1 (I2mean) is used for the calculation

The calculation of (IRMS) despite missing V_1 allows the CPU an emergency mode.

Formulas:

$$(\text{IRMS}) = \frac{\pi}{2\sqrt{2}} \times (\text{I1mean}) = \frac{\pi}{2\sqrt{2}} \times \frac{\sum_{n=0}^{4095} |I_{1n}|}{4096} \text{ [steps]} \qquad \text{I2GTI1FG = 0}$$

$$(\text{IRMS}) = \frac{\pi}{2\sqrt{2}} \times (\text{I2mean}) = \frac{\pi}{2\sqrt{2}} \times \frac{\sum_{n=0}^{4095} |I_{2n}|}{4096} \text{ [steps]} \qquad \text{I2GTI1FG = 1}$$

NOTE: The factor $\pi/(2\sqrt{2})$ (1.11072) converts the mean value of a sine wave to the RMS value.

VPEAK: V_1 Peak Voltage

The value in VPEAK is the absolute maximum ADC value for V_1 measured during the last mains period. The existing V_1 peak value is overwritten only if three larger contiguous samples are taken. The offset corrected value in WAVEFSV1 is used for the comparison.

Format	Unsigned integer	+15.0
Range	0x00 to 0x07FFF	0 to +32,767
Resolution	1 step = 1 k_{V1}	

Formula:

$$v1_{peak} = k_{V1} \times (\text{VPEAK}) \text{ [V]}$$

IPEAK: I_1 or I_2 Peak Current

The value in IPEAK is the absolute maximum ADC value for I_1 or I_2 measured during the last mains period. The peak values are calculated independently for both I_1 and I_2. The internal peak values are only overwritten if three larger contiguous samples are taken. I2GTI1FG defines which I_x value is written to IPEAK after the leading-edge zero crossing of V_1:

- ❑ I2GTI1FG = 0: Internal I_1 peak value is written to IPEAK
- ❑ I2GTI1FG = 1: Internal I_2 peak value is written to IPEAK

Format	Unsigned integer	+15.0
Range	0x00 to 0x07FFF	0 to +32,767
Resolution	1 step = 1 k_{I1} (or 1 k_{I2})	

Formulas:

I2GTI1FG = 0:

$$i1_{peak} = k_{I1} \times (\text{IPEAK}) \text{ [A]}$$

I2GTI1FG = 1:

$$i2_{peak} = k_{I2} \times (\text{IPEAK}) \text{ [A]}$$

LINECYCLCNT: Line Cycle Count

The number of mains frequency periods is accumulated in LINECYCLCNT. The counter is updated with the leading-edge zero crossing of V_1. (LINECYCLCNT = LINECYCLCNT_HI, LINECYCLCNT_LO = 32-bit value)

Format	Unsigned integer	+32.0
Range	0x00 to 0x0FFFF,FFFF	0 to 4.295E+9
Resolution	1 mains cycle	

Example: LINECYCLCNT contains the value 0xFE,4567 indicating 16,663,911 mains cycles occurred since the last overflow. This is equivalent to 92 hours, 34 minutes and 38 seconds for f_{mains} = 50 Hz.

NMBMEAS: ADC Conversion Count

The counter NMBMEAS accumulates the number of measurements since last being cleared by the CPU or ESP430 depending on MB. NMBMEAS increments at the rate given by f_{ADC}.

- ❑ MB = 0: NMBMEAS counts up with each measurement and rolls over after reaching 0xFFFF,FFFF. Counting restarts at zero.
- ❑ MB = 1: When NMBMEAS reaches the value stored in INTRPTLEVL, ILREACHEDFG is set. Counting restarts at zero.

Format	Unsigned integer	+32.0
Range	0x0 to 0x0FFFF,FFFF	0 to 4.295E+9
Resolution	1 measurement	

1.2.14 ESP430CE1A Calibration

Single and dual point meter calibration is possible using the ESP430. When single point calibration is used, the slope (GAINCORR1 and GAINCORR2) is calibrated. When dual point calibration is required, the offset (POFFSET1 and POFFSET2) is calculated in addition to the slope.

In order to determine the slope and offset constants for a given meter, two calibration methodologies are implemented in the ESP430:

- ❑ Calibration over a defined number of mains periods. (Calibration Mode)
- ❑ Calibration using continuous measurements. (Measurement Mode)

Calibration over a defined number of mains periods

This calibration method uses the internal calculations for the products of WAVEFSV1*WAVEFSI1 and WAVEFSV1*WAVEFSI2. These numbers are 16 times smaller than the energy values in ACTENERGY1 and ACTENERGY2. The values in ACTENERGY1 and ACTENERGY2 are adapted to the meter constants C_{Z1} and C_{Z2}. The smaller energy results allow for a longer calibration execution time.

The calibration sequence is given by the following flow:

- ❏ Configure CURR_I2 according to the desired configuration.
- ❏ Parameter registers are initialized for the load point measured by the CPU
- ❏ The ESP430 is set to Calibration mode by the CPU
- ❏ Calibration begins on the next leading-edge zero crossing of V_1. After measurement for the number of mains periods defined by CALCYCLCNT, the calculated active energy is stored in ACTENERGY1 and ACTENERGY2.
- ❏ The flag CALRDY is set indicating the available measurement results.

The same flow is repeated for the second calibration point if required.

Formulas

Calibration is performed during CALCYCCNT mains periods with the two currents I_{1HI} and I_{1LO}. The nominal energy results for the two calibration points are:

$$n_{HIcalc} = C_{Z1} \times I_{1HI} \times V_1 \times PF \times \frac{(CALCYCCNT)}{f_{MAINS}} \times \frac{f_{ADC}}{2^{16}} \left[steps^2\right]$$

$$n_{LOcalc} = C_{Z1} \times I_{1LO} \times V_1 \times PF \times \frac{(CALCYCCNT)}{f_{MAINS}} \times \frac{f_{ADC}}{2^{16}} \left[steps^2\right]$$

The resulting values for the slope and offset are:

Slope:

$$(GAINCORR1) = \frac{n_{HIcalc} - n_{LOcalc}}{n_{HImeas} - n_{LOmeas}} \times 2^{14}$$

Offset:

$$(POFFSET1) = \frac{n_{HImeas} \times n_{LOcalc} - n_{LOmeas} \times n_{HIcalc}}{n_{HImeas} - n_{LOmeas}} \times \frac{f_{MAINS}}{(CALCYCCNT)} \times \frac{2^{16}}{f_{ADC}}$$

Where:
n_{HIcalc} Calculated energy at the high current calibration point [steps^2]
n_{HImeas} Measured energy at the high current calibration point [steps^2]
n_{LOcalc} Calculated energy at the low current calibration point [steps^2]
n_{LOmeas} Measured energy at the low current calibration point [steps^2]

The above formulas shown for I_1 are also valid for I_2. For single point calibration, the “LO” parameters should be set to 0 in the gain correction equation.

Example

The I_1 path is calibrated with the following values (meter constants are assumed):

V_1 = 230 V
I_{1HI} = 20 A, I_{1LO} = 1 A
PF = 1.0
CALCYCCNT = 20
f_{ADC} = 4096 Hz, f_{mains} = 50 Hz

The nominal measurement results n_{HIcalc} and n_{LOcalc} are:

$$n_{HIcalc} = 29,322.80806 \times 20.0 \times 230 \times 1.0 \times \frac{20}{50} \times \frac{4096}{2^{16}} =$$
$$= 3,372,122.927 = 0x0033,745B \left[\text{steps}^2\right]$$
$$n_{LOcalc} = 29,322.80806 \times 1.0 \times 230 \times 1.0 \times \frac{20}{50} \times \frac{4096}{2^{16}} =$$
$$= 168,606.146 = 0x0002,929E \left[\text{steps}^2\right]$$

The measurement results for the two calibration points I_{1LO} and I_{1HI} are:

$n_{1HImeas}$ = 0x32,F0A2 (−1.0 % error compared to $n_{1HIcalc}$ = 0x33,745B)

$n_{1LOmeas}$ = 0x2,9FCA (+2.0 % error compared to $n_{1LOcalc}$ = 0x2,929E)

For the above results, the rounded slope written to GAINCORR1 is:

$$(\text{GAINCORR1}) = \frac{0x0033,745B - 0x0002,929E}{0x0032,F0A2 - 0x0002,9FCA} \times 2^{14} =$$
$$= 1.01171 \times 2^{14} = 0x40C0$$

The offset written to POFFSET1 is:

$$(\text{POFFSET1}) = \frac{0x32,F0A2 \times 0x2,929E - 0x2,9FCA \times 0x33,745B}{0x32,F0A2 - 0x2,9FCA} \times \frac{50}{20} \times \frac{2^{16}}{4096} =$$
$$= -215,465 = 0xFFFC,B657$$

The calculated value in POFFSET1 is the offset for each product WAVEFSV1*WAVEFSI1 and ranges from -2^{30} to $+2^{30}$ (-10^9 to $+10^9$).

If the measured calibration points are corrected with the calculated slope and offset:

$$n_{corr} = (n_{meas} \times (\text{GAINCORR1})) \times 2^{-14} + (\text{P1OFFSET}) \times \frac{\text{CALCYCCNT}}{f_{MAINS}} \times \frac{f_{ADC}}{2^{16}}$$

$$n_{HIcorr} = 0x32,F0A2 \times 0x40C0 \times 2^{-14} + 0xFFFC,B657 \times \frac{20}{50} \times \frac{4096}{2^{16}} =$$

$$= 3,372,137 = 0x0033,7469$$

$$n_{LOcorr} = 0x2,9FCA \times 0x40C0 \times 2^{-14} + 0xFFFC,B657 \times \frac{20}{50} \times \frac{4096}{2^{16}} =$$

$$= 168,607 = 0x2,929F$$

The resulting error for both corrections is $+4.2 \times 10^{-6}$ or 4.2 ppm.

Calibration using continuous measurements

The CPU initializes the ESP430 for normal measurement (Measure mode). The energy values written after each mains period to ACTENSPER1 (and ACTENSPER2 if enabled) can be converted by the CPU into a proportional, constant output frequency containing information for the mean value of the measured energy. Timer_A may be used for the generation of the energy-proportional output frequency.

The calibration sequence is (repeat for two-point calibration):

- ❏ Configure CURR_I2 according to the desired configuration.
- ❏ Parameter registers are initialized for the load point measured by the CPU
- ❏ The ESP430 is set to Measure mode by the CPU
- ❏ The 1st result in ACTENSPER1 (and ACTENSPER2 if enabled) should be ignored, due to the possibility of calculating over a partial mains period. Each subsequent result in ACTENSPER1 (and ACTENSPER2) is used for the calculations for the required number of mains cycles.
- ❏ Energy results for the last mains period are available in ACTENSPER1 and ACTENSPER2. This is indicated by ZXLDFG and WFSRDYFG.
- ❏ The CPU resets WFSRDYFG and processes the results with the equations below.

Formulas

Calibration is performed for a single or multiple mains periods with the two currents I_{1HI} and I_{1LO}. The nominal energy results for the two calibration points are:

$$n_{HIcalc} = C_{Z1} \times I_{1HI} \times V_1 \times PF \times \frac{(CALCYCCNT)}{f_{MAINS}} \times \frac{f_{ADC}}{4096} \left[steps^2\right]$$

$$n_{LOcalc} = C_{Z1} \times I_{1LO} \times V_1 \times PF \times \frac{(CALCYCCNT)}{f_{MAINS}} \times \frac{f_{ADC}}{4096} \left[steps^2\right]$$

The resulting values for the slope and offset are:

Slope:

$$(GAINCORR1) = \frac{n_{HIcalc} - n_{LOcalc}}{n_{HImeas} - n_{LOmeas}} \times 2^{14}$$

Offset:

$$(POFFSET1) = \frac{n_{HImeas} \times n_{LOcalc} - n_{LOmeas} \times n_{HIcalc}}{n_{HImeas} - n_{LOmeas}} \times \frac{f_{MAINS}}{(CALCYCCNT)} \times \frac{4096}{f_{ADC}}$$

Example

I_1 is calibrated with the following values (meter constants are assumed):

V_1 = 230 V
I_{1HI} = 20 A, I_{1LO} = 1 A
PF = 1.0
CALCYCCNT = 1
f_{ADC} = 2048 Hz, f_{mains} = 50 Hz

The nominal measurement results n_{HIcalc} and n_{LOcalc} are:

$$n_{HIcalc} = 29,322.80806 \times 20.0 \times 230 \times 1.0 \times \frac{1}{50} \times \frac{2048}{4096} =$$

$$= 1,348,849.171 = 0x14,94F1 \left[\text{steps}^2\right]$$

$$n_{LOcalc} = 29,322.80806 \times 1.0 \times 230 \times 1.0 \times \frac{1}{50} \times \frac{2048}{4096} =$$

$$= 67,442.458 = 0x1,0772$$

The measurement results for the two calibration points I_{1LO} and I_{1HI} are:

$n_{1HImeas}$ = 0x14,6040 (−1.0 % error compared to $n_{1HIcalc}$ = 0x14,94F1)

$n_{1LOmeas}$ = 0x1,0CB7 (+2.0 % error compared to $n_{1LOcalc}$ = 0x1,0772)

With the above results the rounded slope in GAINCORR1 is:

$$(\text{GAINCORR1}) = \frac{0x14,94F1 - 0x1,0772}{0x14,6040 - 0x1,0CB7} \times 2^{14} =$$

$$= 1.01171 \times 2^{14} = 0x40C0$$

The offset in P1OFFSET1 is:

$$(\text{POFFSET1}) = \frac{0x14,6040 \times 0x1,0772 - 0x1,0CB7 \times 0x14,94F1}{0x14,6040 - 0x2,9FCA} \times \frac{50}{1} \times \frac{4096}{2048} =$$

$$= -215,489 = 0xFFFC,B63F$$

If the measured calibration points are corrected with the calculated slope and offset:

$$n_{corr} = (n_{meas} \times (\text{GAINCORR1})) \times 2^{-14} + (\text{P1OFFSET}) \times \frac{\text{CALCYCCNT}}{f_{MAINS}} \times \frac{f_{ADC}}{4096}$$

$$n_{HIcorr} = 0x14,6040 \times 0x40C0 \times 2^{-14} + 0xFFFC,B63F \times \frac{1}{50} \times \frac{2048}{4096} =$$

$$= 1,348,890 = 0x0014,951A$$

$$n_{LOcorr} = 0x1,0CB7 \times 0x40C0 \times 2^{-14} + 0xFFFC,B63F \times \frac{1}{50} \times \frac{2048}{4096} =$$

$$= 67,441 = 0x1,0771$$

The resulting error for both corrections is $+3.1X10^{-5}$ or 31 ppm.

When compared to calibration over a defined number of mains periods, the larger resulting error for calibration using continuous measurements is due to the smaller return register results caused by measurement over only one mains period. Using additional cycles will minimize this error.

1.3 ESP430CE1(A) Registers

The ESP430 registers are listed in Table 1−13, Table 1−14, and Table 1−15.

Table 1−13. Control Registers

Register	Short Form	Register Type	Address	Initial State
ESP430CE1 Control	ESPCTL	Read/write	0150h	Reset with PUC
Mailbox Control	MBCTL	Read/write	0152h	Reset with PUC
Incoming Mailbox 0	MBIN0	Read	0154h	Reset with PUC
Incoming Mailbox 1	MBIN1	Read	0156h	Reset with PUC
Outgoing Mailbox 0	MBOUT0	Write	0158h	Reset with PUC
Outgoing Mailbox 1	MBOUT1	Write	015Ah	Reset with PUC

Table 1−14. Parameter Registers

Register	Short Form	Register Type	Address†	Initial State
ESP430 Control 0	ESP430_CTRL0	Read/write	N/A	Reset with PUC
Event Message Enable	EVENT	Read/write	N/A	Reset with PUC
I_1 Phase Correction	PHASECORR1	Read/write	N/A	Reset with PUC
I_2 Phase Correction	PHASECORR2	Read/write	N/A	Reset with PUC
V_1 Offset Correction	V1OFFSET	Read/write	N/A	Reset with PUC
I_1 Offset Correction	I1OFFSET	Read/write	N/A	Reset with PUC
I_2 Offset Correction	I2OFFSET	Read/write	N/A	Reset with PUC
I_1 Adaptation Factor	ADAPTI1	Read/write	N/A	Reset with PUC
I_2 Adaptation Factor	ADAPTI2	Read/write	N/A	Reset with PUC
V_1 x I_1 Gain Correction	GAINCORR1	Read/write	N/A	Reset with PUC
V_1 x I_1 Offset Correction LSW	POFFSET1_LO	Read/write	N/A	Reset with PUC
V_1 x I_1 Offset Correction MSW	POFFSET1_HI	Read/write	N/A	Reset with PUC
V_1 x I_2 Gain Correction	GAINCORR2	Read/write	N/A	Reset with PUC
V_1 x I_2 Offset Correction LSW	POFFSET2_LO	Read/write	N/A	Reset with PUC
V_1 x I_2 Offset Correction MSW	POFFSET2_HI	Read/write	N/A	Reset with PUC
Energy Overflow LSW	INTRPTLEVL_LO	Read/write	N/A	Reset with PUC
Energy Overflow MSW	INTRPTLEVL_HI	Read/write	N/A	Reset with PUC
Calibration Cycle Count	CALCYCLCNT	Read/write	N/A	Reset with PUC
I_1, I_2 Meter Threshold LSW	STARTCURR_FRAC	Read/write	N/A	Reset with PUC
I_1, I_2 Meter Threshold MSW	STARTCURR_INT	Read/write	N/A	Reset with PUC
Mains Nominal Frequency	NOMFREQ	Read/write	N/A	Reset with PUC
V_1 Drop Cycle Counter	VDROPCYCLS	Read/write	N/A	Reset with PUC
I_1:I_2 Tamper Ratio	RATIOTAMP	Read/write	N/A	Reset with PUC
I_1 I_2 Tamper Level	ITAMP	Read/write	N/A	Reset with PUC
V_1 Drop Level Threshold	VDROPLEVEL	Read/write	N/A	Reset with PUC
V_1 Peak Level Threshold	VPEAKLEVEL	Read/write	N/A	Reset with PUC

† All parameter registers are accessed using the mailbox registers and are not mapped within the memory space of the CPU.

Table 1−14. Parameter Registers (continued)

Register	Short Form	Register Type	Address†	Initial State
I_1, I_2 Peak Level Threshold	IPEAKLEVEL	Read/write	N/A	Reset with PUC
DC Removal Period Count	DCREMPER	Read/write	N/A	Reset with PUC
	DELTAV1MAX‡	Read/write	N/A	Reset with PUC
	CMRRCOMP‡	Read/write	N/A	Reset with PUC
	FADCU‡	Read/write	N/A	Reset with PUC

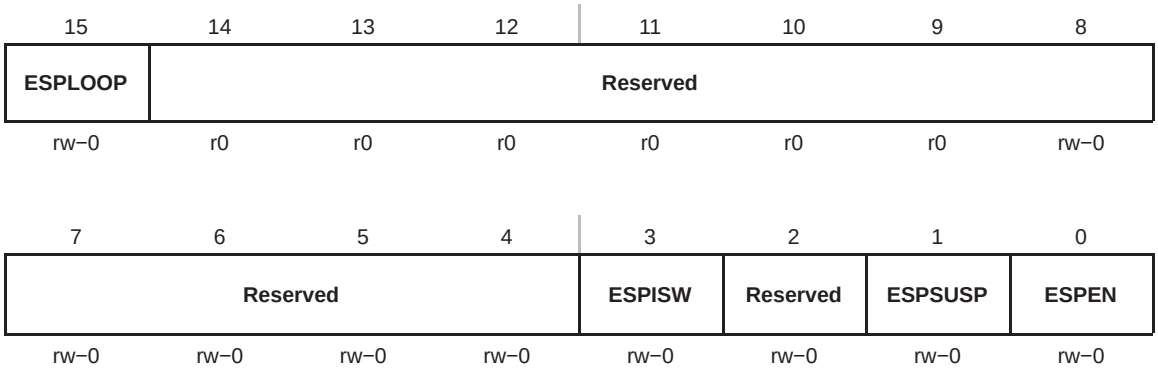
† All parameter registers are accessed using the mailbox registers and are not mapped within the memory space of the CPU.
‡ Present only in devices with the ESP430CE1A.

Table 1−15. Return Registers

Register	Short Form	Register Type	Address	Initial State
ESP430 Status 0	ESP430_STAT0	Read	01C0h	Reset with PUC
ESP430 Status 1†	ESP430_STAT1	Read	01C2h	Reset with PUC
V_1 Waveform Sample	WAVEFSV1	Read	01C4h	Reset with PUC
I_1 Waveform Sample	WAVEFSI1	Read	01CAh	Reset with PUC
I_2 Waveform Sample	WAVEFSI2	Read	01CCh	Reset with PUC
I_1 Active Energy LSW	ACTENERGY1_LO	Read	01D0h	Reset with PUC
I_1 Active Energy MSW	ACTENERGY1_HI	Read	01D2h	Reset with PUC
I_2 Active Energy LSW	ACTENERGY2_LO	Read	01D4h	Reset with PUC
I_2 Active Energy MSW	ACTENERGY2_HI	Read	01D6h	Reset with PUC
Reactive Energy LSW	REACTENERGY_LO	Read	01D8h	Reset with PUC
Reactive Energy MSW	REACTENERGY_HI	Read	01DAh	Reset with PUC
Apparent Energy LSW	APPENERGY_LO	Read	01DCh	Reset with PUC
Apparent Energy MSW	APPENERGY_HI	Read	01DEh	Reset with PUC
I_1 Active Energy Per Cycle LSW	ACTENPER1_LO	Read	01E0h	Reset with PUC
I_1 Active Energy Per Cycle MSW	ACTENPER1_HI	Read	01E2h	Reset with PUC
I_2 Active Energy Per Cycle LSW	ACTENPER2_LO	Read	01E4h	Reset with PUC
I_2 Active Energy Per Cycle MSW	ACTENPER2_HI	Read	01E6h	Reset with PUC
Power Factor	POWERFCT	Read	01E8h	Reset with PUC
Capacitive/Inductive Cycle Counter	CAPIND	Read	01EAh	Reset with PUC
Mains Line Cycle Period	MAINSPERIOD	Read	01ECh	Reset with PUC
V_1 RMS Result	V1RMS	Read	01EEh	Reset with PUC
I_x RMS LSW Result	IRMS_LO	Read	01F0h	Reset with PUC
I_x RMS MSW Result	IRMS_HI	Read	01F2h	Reset with PUC
V_1 Peak Result	VPEAK	Read	01F4h	Reset with PUC
I_x Peak Result	IPEAK	Read	01F6h	Reset with PUC
Line Cycle Counter LSW Result	LINECYCLCNT_LO	Read	01F8h	Reset with PUC
Line Cycle Counter MSW Result	LINECYCLCNT_HI	Read	01FAh	Reset with PUC
Measurement Counter LSW Result	NMBMEAS_LO	Read	01FCh	Reset with PUC
Measurement Counter MSW Result	NMBMEAS_HI	Read	01FEh	Reset with PUC

† Present only in devices with the ESP430CE1A

ESPCTL, ESP430 Control Register



ESPLOOP Bit 15 Loop-back enable. Allows writing to the normally “read-only” return registers when EN = 0.
0 Loop mode disabled
1 Loop mode enabled

Reserved Bits 14-4 Reserved

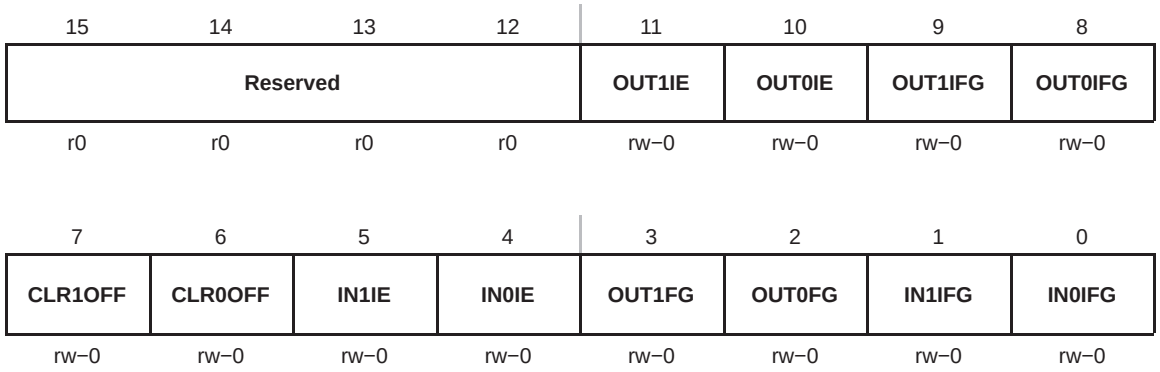
ESPISW Bit 3 Interrupt switch enable. This bit controls the routing of shared module interrupts (SD16 and hardware multiplier) when ESPSUSP = 1. Modifying ESPISW clears the interrupt enable bits of each shared module.
0 Interrupts routed to the ESP430 and serviced when ESPSUSP = 0
1 Interrupts routed to the CPU

Reserved Bit 2 Reserved

ESPSUSP Bit 1 ESP430 module suspend
0 ESP430 is active
1 ESP430 activity is halted

ESPEN Bit 0 ESP430 module enable
0 ESP430 disabled
1 ESP430 enabled

MBCTL, Mailbox Control Register



Reserved Bits 15-12 Reserved

OUT1IE Bit 11 Outgoing Mailbox 1 interrupt enable
0 Interrupt disabled
1 Interrupt enabled

OUT0IE Bit 10 Outgoing Mailbox 0 interrupt enable
0 Interrupt disabled
1 Interrupt enabled

OUT1IFG Bit 9 Outgoing Mailbox 1 interrupt flag. This bit is set when OUT1FG is cleared indicating the message in MBOUT1 has been processed by the ESP430. OUT1IFG is cleared when a message is written to MBOUT1 or by software.
0 No interrupt pending
1 Interrupt pending

OUT0IFG Bit 8 Outgoing Mailbox 0 interrupt flag. This bit is set when OUT0FG is cleared indicating the message in MBOUT0 has been processed by the ESP430. OUT0IFG is cleared when a message is written to MBOUT0 or by software.
0 No interrupt pending
1 Interrupt pending

CLR1OFF Bit 7 Incoming Mailbox 1 interrupt flag auto-clear disable.
0 IN1IFG is automatically cleared when MBIN1 is read by the CPU
1 IN1IFG must be cleared in software by the CPU

CLR0OFF Bit 6 Incoming Mailbox 0 interrupt flag auto-clear disable.
0 IN0IFG is automatically cleared when MBIN0 is read by the CPU
1 IN0IFG must be cleared in software by the CPU

IN1IE Bit 5 Incoming Mailbox 1 interrupt enable
0 Interrupt disabled
1 Interrupt enabled

IN0IE	Bit 4	Incoming Mailbox 0 interrupt enable 0 Interrupt disabled 1 Interrupt enabled
OUT1FG	Bit 3	Outgoing Mailbox 1 flag. This bit is set when a message is written to MBOUT1 and is cleared after it has been processed by the ESP430.
OUT0FG	Bit 2	Outgoing Mailbox 0 flag. This bit is set when a message is written to MBOUT0 and is cleared after it has been processed by the ESP430.
IN1IFG	Bit 1	Incoming Mailbox 1 interrupt flag. This bit is set when a new message is available in MBIN1. 0 No interrupt pending 1 Interrupt pending
IN0IFG	Bit 0	Incoming Mailbox 0 interrupt flag. This bit is set when a new message is available in MBIN0. 0 No interrupt pending 1 Interrupt pending

MBIN0, Incoming Command Mailbox Register

15	14	13	12	11	10	9	8
Incoming Command							
r−0	r−0	r−0	r−0	r−0	r−0	r−0	r−0

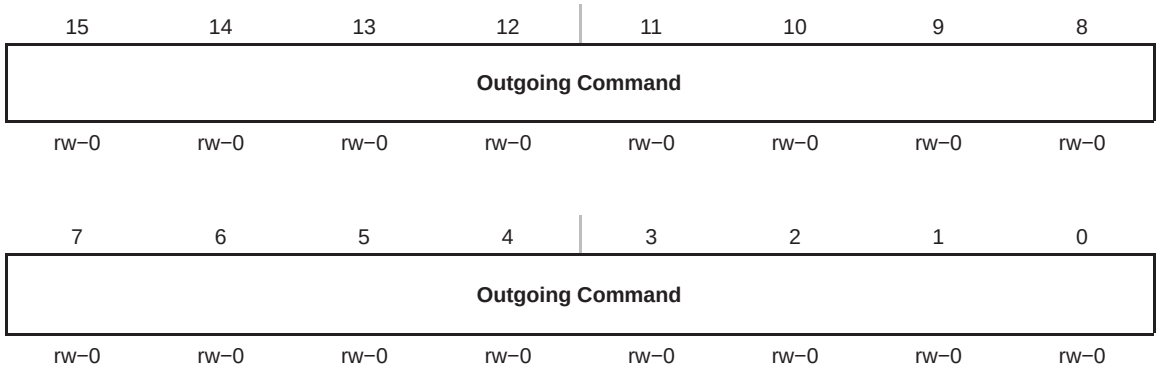
7	6	5	4	3	2	1	0
Incoming Command							
r−0	r−0	r−0	r−0	r−0	r−0	r−0	r−0

MBIN1, Incoming Data Mailbox Register

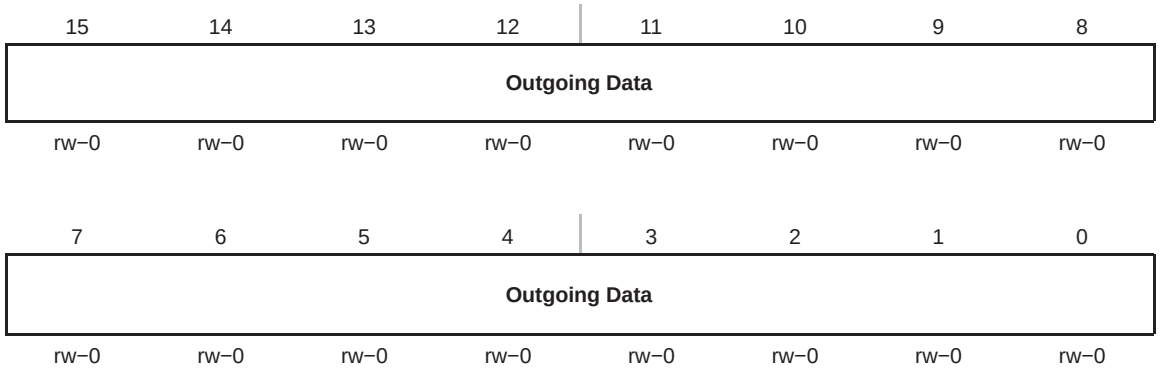
15	14	13	12	11	10	9	8
Incoming Data							
r−0	r−0	r−0	r−0	r−0	r−0	r−0	r−0

7	6	5	4	3	2	1	0
Incoming Data							
r−0	r−0	r−0	r−0	r−0	r−0	r−0	r−0

MBOUT0, Outgoing Command Mailbox Register



MBOUT1, Outgoing Data Mailbox Register



ESP430_CTRL0, ESP430 Control Parameter Register

15	14	13	12	11	10	9	8
Reserved						I2CMRR†	V1FILTER†
rw−0	rw−0	rw−0	rw−0	rw−0	rw−0	rw−0	rw−0

7	6	5	4	3	2	1	0
DCREM_I2	DCREM_I1	DCREM_V1	NE1	NE0	MB	CURR_I1	CURR_I2
rw−0	rw−0	rw−0	rw−0	rw−0	rw−0	rw−0	rw−0

† Present only in devices with the ESP430CE1A. Reserved in other devices.

Reserved Bits 15-10 Reserved

I2CMRR Bit 9 Switches the common-mode rejection function for current I2.
0 Disabled
1 Enabled

V1FILTER Bit 8 Switches the spike filter function for voltage V1
0 Disabled
1 Enabled

DCREM_I2 Bit 7 I_2 DC removal algorithm enable
0 Disabled
1 Enabled

DCREM_I1 Bit 6 I_1 DC removal algorithm enable
0 Disabled
1 Enabled

DCREM_V1 Bit 5 V_1 DC removal algorithm enable
0 Disabled
1 Enabled

NEx Bits 4-3 Negative active energy control select
00 Negative active energy is set to zero
01 Absolute active energy is used by ESP430
10 Negative active energy is used by ESP430
11 Reserved

MB Bit 2 Energy threshold select
0 INTRPTLEVL = energy level
1 INTRPTLEVL = measurement count

CURR_I1 Bit 1 I_1 current channel sensor select
0 I_1 active
1 Reserved

CURR_I2 Bit 0 I_2 current channel enable
0 I_2 disabled
1 I_2 active

EVENT, ESP430 Event Message Enable Parameter Register

15	14	13	12	11	10	9	8
ACTIVEME	**Reserved**		**I2PEAKME**	**I1PEAKME**	**VPEAKME**	**VDROPME**	**NEGENME**
rw−0	rw−0	rw−0	rw−0	rw−0	rw−0	rw−0	rw−0

7	6	5	4	3	2	1	0
TAMPME	**CALRDYME**	**ZXTRME**	**ZXLDME**	**ENRDYME**	**IL REACHED ME**	**I2GTI1ME**	**WFSRDY ME**
rw−0	rw−0	rw−0	rw−0	rw−0	rw−0	rw−0	rw−0

ACTIVEME Bit 15 ACTIVEFG message enable
0 Disabled
1 Enabled

Reserved Bits 14-13 Reserved

I2PEAKME Bit 12 I2PEAKFG message enable
0 Disabled
1 Enabled

I1PEAKME Bit 11 I1PEAKFG message enable
0 Disabled
1 Enabled

VPEAKME Bit 10 VPEAKFG message enable
0 Disabled
1 Enabled

VDROPME Bit 9 VDROPFG message enable
0 Disabled
1 Enabled

NEGENME Bit 8 NEGENFG message enable
0 Disabled
1 Enabled

TAMPME Bit 7 TAMPFG message enable
0 Disabled
1 Enabled

CALRDYME Bit 6 CALRDYFG message enable
0 Disabled
1 Enabled

ZXTRME Bit 5 ZXTRFG message enable
0 Disabled
1 Enabled

ZXLDME	Bit 4	ZXLDFG message enable 0 Disabled 1 Enabled
ENRDYME	Bit 3	ENRDYFG message enable 0 Disabled 1 Enabled
IL REACHED ME	Bit 2	ILREACHEDFG message enable 0 Disabled 1 Enabled
I2GTI1ME	Bit 1	I2GTI1FG message enable 0 Disabled 1 Enabled
WFSRDY ME	Bit 0	WFSRDYFG message enable 0 Disabled 1 Enabled

Note: Remaining Parameter Registers

Definitions for the remaining Parameter registers are given in the ESP430CE1 Parameter Register Description section of this guide. These registers represent 8-bit or 16-bit values and do not contain individual bit definitions.

ESP430_STAT0, ESP430 Status Return Register 0

15	14	13	12	11	10	9	8
ACTIVEFG	**Reserved**		**I2PEAKFG**	**I1PEAKFG**	**VPEAKFG**	**VDROPFG**	**NEGENFG**
r−0	r−0	r−0	r−0	r−0	r−0	r−0	r−0

7	6	5	4	3	2	1	0
TAMPFG	**CALRDYFG**	**ZXTRFG**	**ZXLDFG**	**ENRDYFG**	**ILREA-CHEDFG**	**I2GTI1FG**	**WFSRDYFG**
r−0	r−0	r−0	r−0	r−0	r−0	r−0	r−0

ACTIVEFG Bit 15 ESP430 status flag
0 ESP430 is in IDLE mode
1 ESP430 is in ACTIVE mode

Reserved Bits 14-13 Reserved

I2PEAKFG Bit 12 I_2 over-current flag. I2PEAKFG is set when the peak I_2 current measured exceeds IPEAKLEVEL for three or more consecutive samples.
0 Line normal
1 Line overcurrent detected

I1PEAKFG Bit 11 I_1 over-current flag. I1PEAKFG is set when the peak I_1 current measured exceeds IPEAKLEVEL for three or more consecutive samples.
0 Line normal
1 Line over-current detected

VPEAKFG Bit 10 V_1 over-voltage flag. VPEAKFG is set when the peak V_1 voltage measured exceeds VPEAKLEVEL for three or more consecutive samples.
0 Line normal
1 Line over-voltage detected

VDROPFG Bit 9 V_1 under-voltage flag. VDROPFG is set when the peak V_1 voltage measured is less than VDROPLEVEL for the number of consecutive mains cycles defined by VDROPCYCLS.
VDROPFG is also set if V1RMS is less than 0.088 x VDROPLEVEL to insure notification if V_1= 0 and no zero crossings occur. Maximum response time is 2 seconds.
0 Line normal
1 Line under-voltage detected

NEGENFG Bit 8 Negative energy flag. Negative energy sum calculated over the last 4096 samples.
- 0 Event message sent if NEGENME = 1 or CLR_EVENT command issued by CPU
- 1 Negative energy detected

TAMPFG Bit 7 Tampered meter flag. Tamper detection is monitored at a frequency of $f_{ADC}/4096$ (e.g., 1Hz for f_{ADC} = 4096).
- 0 Normal operation
- 1 Potential tamper condition detected

CALRDYFG Bit 6 Calibration ready flag.
- 0 Event message sent if CALRDYME = 1, CLR_EVENT command issued by CPU or ESP430 set into Idle mode.
- 1 Calibration cycle complete, new values ready in ACTENERGYx.

ZXTRFG Bit 5 V_1 zero crossing, trailing-edge flag (negative-going zero crossing).
- 0 Leading-edge zero crossing occurred
- 1 Trailing edge zero crossing occurred

ZXLDFG Bit 4 V_1 zero crossing, leading-edge flag (positive-going zero crossing).
- 0 Trailing-edge zero crossing occurred
- 1 Leading-edge zero crossing occurred

ENRDYFG Bit 3 Energy ready flag. Indicates update of V1RMS, IRMS, ACTENERGYx, REACTENERGY, APPENERGY, POWERFCT and CAPIND registers.
- 0 Event message sent if ENRDYME = 1 or CLR_EVENT command issued by CPU
- 1 Updated results available

ILREA-CHEDFG Bit 2 Interrupt energy level reached flag.
- 0 Event message sent if ILREACHEDME = 1 or CLR_EVENT command issued by CPU
- 1 Interrupt level reached as defined by MB and INTRPTLEVL

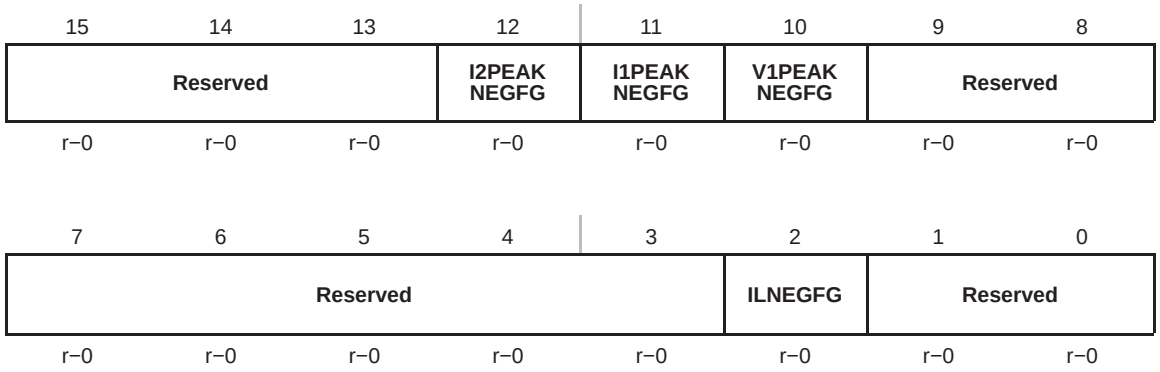
I2GTI1FG Bit 1 I_2 greater than I_1 flag.
- 0 I_1 RMS > I_2 RMS during last 4096 measurements
- 1 I_2 RMS > I_1 RMS during last 4096 measurements

WFSRDYFG Bit 0 Waveform samples ready flag. Indicates update of WAVEFSV1 and WAVEFSIx registers. Values are offset-corrected and updated at f_{ADC}.
- 0 Event message sent if WFSRDYME = 1 or CLR_EVENT command issued by CPU
- 1 Updated results available

Note: Remaining Return Registers

Definitions for the remaining Return registers are given in the ESP430CE1 Return Register Description section of this guide. These registers represent 8-bit or 16-bit values and do not contain individual bit definitions.

ESP430_STAT1, ESP430 Status Return Register 1†



† Present only in devices with the ESP430CE1A

Reserved	Bits 15−13	Reserved
I2PEAK NEGFG	Bit 12	Indicates the sign of the measured I_2 peak. I2PEAKNEGFG = 0: Last I_2 peak was positive I2PEAKNEGFG = 1: Last I_2 peak was negative The bit is not reset by sending an event message or with the command CLR_EVENT.
I1PEAK NEGFG	Bit 11	Indicates the sign of the measured I_1 peak. I1PEAKNEGFG = 0: Last I_1 peak was positive I1PEAKNEGFG = 1: Last I_1 peak was negative The bit is not reset by sending an event message or with the command CLR_EVENT.
V1PEAK NEGFG	Bit 10	Indicates the sign of the measured V_1 peak. V1PEAKNEGFG = 0: Last V_1 peak was positive V1PEAKNEGFG = 1: Last V_1 peak was negative The bit is not reset by sending an event message or with the command CLR_EVENT.
Reserved	Bits 9−3	Reserved
ILNEGFG	Bit 2	Indicates the sign of the energy of the reached Interrupt Level. ILNEGFG = 0: energy is positive ILNEGFG = 1:energy is negative Set if the energy of the reached interrupt level is negative. Reset if the energy of the reached interrupt level is positive. It is not reset by sending an event message or with the command CLR_EVENT.
Reserved	Bits 1−0	Reserved

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Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
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