

# A Glossary of Analog-to-Digital Specifications and Performance Characteristics

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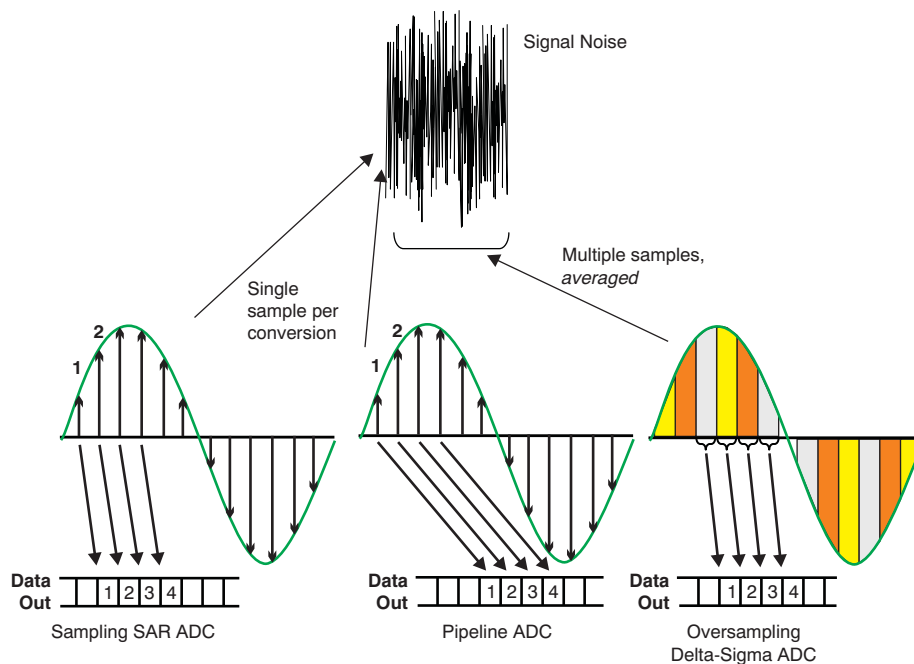
## ABSTRACT

This glossary is a collection of the definitions of Texas Instruments' Delta-Sigma ( $\Delta\Sigma$ ), successive approximation register (SAR), and pipeline analog-to-digital (A/D) Converter specifications and performance characteristics. Although there is a considerable amount of detail in this document, the product data sheet for a particular product specification is the best and final reference. To download or view a specific data converter product data sheet, see the Texas Instruments web site at [www.ti.com/](http://www.ti.com/).

## Glossary of Terms

### Acquisition Time:

Refer to [Figure 1](#) when comparing SAR, Pipeline, and Delta-Sigma converter acquisition time.



**Figure 1. SAR vs Pipeline vs  $\Delta\Sigma$  A/D Converters Sampling Algorithms Comparison**

- Acquisition time, Delta-Sigma A/D Converters—**

The Delta-Sigma ( $\Delta\Sigma$ ) converter *averages* multiple samples for each conversion result. The *averaging* performed by the converter usually occurs in the form of a Finite Impulse Response (FIR) or Infinite Impulse Response (IIR) digital filter. Consequently, the acquisition time is longer than it is with a SAR or pipeline converter, which only samples the signal once for each conversion. [Figure 1](#) illustrates one of the differences between the sampling mechanism of a SAR, a Pipeline and a  $\Delta\Sigma$  converter. If the user presents a step-input to the delta-sigma converter input or switches a multiplexer output channel,

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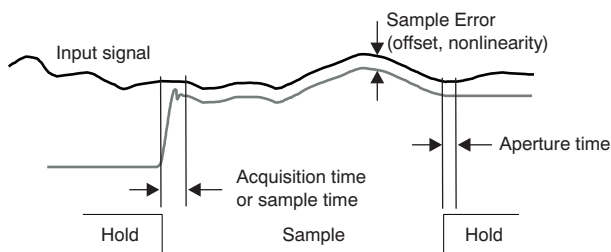
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the converter will require time for the digital filter to refresh with the new signal. If a *snap-shot* of the signal or a defined acquisition point in time is required, it is more appropriate to use a SAR A/D converter.

- **Acquisition time, Pipeline A/D Converters–**

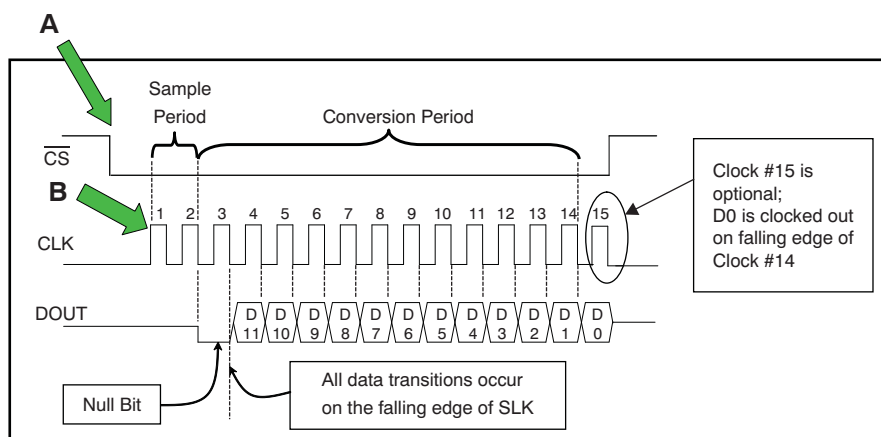
With a pipeline A/D converter, the user initiates the conversion process with the rising edge (or falling edge, as specified in the product data sheet) of the external input clock. The capture of the differential input signal follows the opening of the input internal switches. See [Figure 1](#) and [Figure 2](#).



**Figure 2. Acquisition Time (Sample Time) and Aperture Time**

- **Acquisition time, SAR A/D Converters–**

The acquisition time for the SAR converter is the time required for the sampling mechanism to capture the input voltage. This time begins after the sample command is given where the hold capacitor charges. Some converters have the capability of sampling the input signal in response to a sampling pin on the converter. Other SAR CMOS converters sample with the clock after  $\overline{CS}$  (chip select) drops (with a serial peripheral interface, or SPI™). [Figure 3](#) shows an example of a clock-initiated sample using the ADS7816. Also see [Figure 1](#) and [Figure 2](#).



A Chip select ( $\overline{CS}$ ) falls.

B The falling edge of the clock closes the sample switch.

**Figure 3. Clock-Initiated Sample for a SAR A/D Converter**

**Analog Input, Analog Bandwidth:** The input frequency where the reconstructed output of the A/D converter is 3dB below the value of the input signal.

**Analog Input, Capacitance, Common-mode:** The common-mode capacitance of an A/D converter is the capacitance between each analog signal input(s) and ground.

**Analog Input, Capacitance, Differential:** The capacitance between the positive input ( $A_{IN+}$ ) and negative input ( $A_{IN-}$ ) of an A/D converter with a differential input.

**Analog Input, Differential Input:** With the analog differential input, both input pins of the A/D converter can swing the full range, and typically change in a balanced fashion—that is, as one input goes up, the other goes down in a corresponding way. The differential input offers the advantage of subtracting the two inputs and provides common-mode rejection. These types of inputs are commonly found in single-supply converters, such as delta-sigma or pipeline converters. The differential input offers the advantages of common-mode rejection, with a smaller input voltage swing required on each pin while preserving a high dynamic range.

**Analog Input, Impedance, Common-mode:** The impedance between each analog signal input of the A/D converter and ground.

**Analog Input, Impedance, Differential:** The impedance between the positive input ( $A_{IN+}$ ) and negative input ( $A_{IN-}$ ) of an A/D converter with a differential input.

**Analog Input, Voltage Range, Absolute:** The absolute analog voltage range of an A/D converter is the maximum and minimum voltage limit of the input stage (compared to ground and/or the analog supply voltage). This term describes the absolute input voltage range limits of the input stage. Usually, the positive and negative power supplies impose these limits on the device, unless there is a resistance network on the input. If there is a resistive input network, the absolute inputs can exceed the positive and negative power supplies.

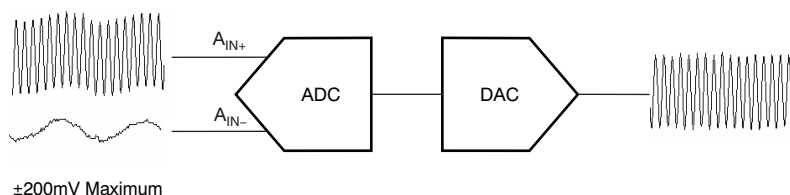
**Analog Input, Voltage Range, Bipolar Input Mode (Differential Inputs):** An A/D converter configured in a Bipolar Input Mode has an input range that uses two input pins and allows negative and positive analog inputs on both pins with respect to each other. In this configuration, neither input pin goes below or above the absolute input voltage range. (See [Input Voltage Range Differential Inputs](#).)

**Analog Input, Voltage Range, Full-Scale (FS or FSR):** The converter digitizes the input signal up to the full-scale input voltage. The internal or external applied voltage reference value determines the full-scale input voltage range. The actual FS input voltage range will vary from device to device. Refer to the specific A/D converter data sheet for details.

- For an ***n*-bit converter**, FS is equal to:  
$$FS = (2^n) \times (\text{ideal code width})$$
- For **delta-sigma converters**, FSR is often used to express units in terms of percentages. For instance, you may find INL defined at  $\pm 0.001\%$  of FSR. In this instance, the input range of the A/D converter could be  $\pm 2.5V$ , with a  $FSR = 5V$ .

Also see: [Analog Inputs, Differential Inputs](#). Refer to a specific A/D converter data sheet for details.

**Analog Input, Voltage Range, Pseudo-differential:** A pseudo-differential input has two input pins,  $A_{IN+}$  and  $A_{IN-}$ , as [Figure 4](#) illustrates. With a pseudo-differential input, the second input pin provides the reference for the signal. This second input pin (the negative input) can only accept a small range of voltages, perhaps a few hundred millivolts (mV). This configuration can be very helpful in situations where the signal has a slight common-mode offset or small-signal error. The pseudo-differential input reduces this offset or small-signal error because the converter sees only the difference between the positive input pin and the negative input pin.



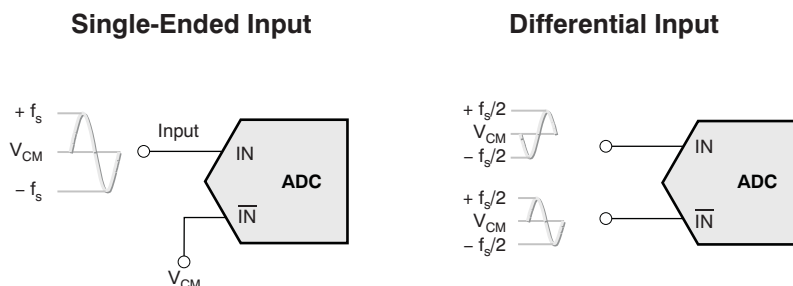
**Figure 4. Pseudo-Differential Mode for A/D Converters**

**Analog Input, Voltage Range, Single-ended (unipolar and bipolar):** A single-ended input A/D converter is configured for one input voltage that is referenced to ground. Some single-supply devices have a single-ended input range that allows only positive analog input signals. Other single-supply (and dual-supply) parts handle a signal that moves both above ground and below ground, and have a bipolar input. Also see [Analog Input, Voltage Range, Pseudo-differential](#).

**Analog Input, Voltage Range, Differential Inputs:** The differential input voltage range is equal to the noninverting analog input ( $A_{IN+}$ ) minus the inverting analog input ( $A_{IN-}$ ). With these two input pins, the input voltage range is:

$$\text{Full-Scale} = ((A_{IN+(MAX)} - A_{IN-(MIN)}) - (A_{IN+(MIN)} - A_{IN-(MAX)}))$$

A positive digital output is produced when the analog input differential voltage ( $A_{IN+} - A_{IN-}$ ) is positive. A negative analog input differential voltage produces negative digital output. Most SAR and delta-sigma A/D converters operate in a similar fashion to analog instrumentation amplifiers and do not require a common-mode voltage. Most CMOS pipeline A/D converters require a common-mode voltage bias ( $V_{CM}$ ) to the inputs, which is typically set to mid-supply ( $+V_S/2$ ). An external source can drive the differential converter inputs in one of two ways: either single-ended or differential. See [Figure 5](#).



**Figure 5. Single-Ended and Differential Inputs to an A/D Converter**

**Analog-to-Digital Converter (ADC, A-D Converter, A/D Converter):** An A/D converter is a device that changes a continuous signal into a discrete-time, discrete-amplitude digitized signal.

#### Aperture:

- **Delay–**

The delay in time between the rising or falling edge (typically the 50% point) of the external sample command and the actual time at which the signal is captured. See [Figure 2](#).

- **Jitter–**

Aperture jitter is the standard deviation of aperture delay from sample to sample over time. Aperture jitter is sometimes mistaken as input noise. The aperture jitter, along with clock jitter of the sampling system, impacts the overall signal-to-noise ratio (SNR) of the conversion. The contribution of jitter to the SNR is equal to:

$$\text{SNR} = 20\log_{10}\left(\frac{1}{(2\pi f t_j)^2}\right)$$

Where:

- $t_j$  is the clock and aperture jitter;
- $f$  is the clock frequency of the converter

The aperture and clock jitter is equal to:

$$t_j = \sqrt{(t_a^2 + t_c^2)}$$

Where:

- $t_a$  is the root-mean-square of the aperture jitter;
- $t_c$  is the root-mean-square of the clock jitter

There is no correlation between the clock-jitter and aperture-jitter terms; therefore, these terms can be combined on a root-sum-square basis (rss).

- **Uncertainty–**Also known as *aperture jitter*.

**Asynchronous Sampling:** Sampling of the A/D converter that is not locked to the frequencies or the time of other frequencies or samples in the application circuit.

**Average Noise Floor:** In a Fast Fourier Transform (FFT) representation of converter data, the average noise floor is a calculated average of all of the bins within the FFT plot, excluding the input signal and signal harmonics.

**Binary Twos Complement Code (BTC):** With the BTC code, the digital zero (0000, for a 4-bit system) corresponds to Bipolar Zero (BPZ), and the digital count increments to its maximum positive code of 0111 as the analog voltage approaches and reaches its positive full-scale value. The code then continues at the negative full-scale value at a digital code of 1000, then approaches BPZ until a digital value of 1111 (for a 4-bit system) is reached at one LSB value below BPZ (see [Table 1](#)). With the BTC coding scheme, the most significant bit (MSB) can also be considered a sign indicator. When the MSB is a logic '0' a positive value is indicated; when the MSB is a logic '1' a negative value is indicated. The analog positive full-scale minus one LSB digital representation is equal to (0111), and the analog negative full-scale representation is (1000). See [Table 1](#) for more details.

**Table 1. BTC Coding Scheme<sup>(1)(2)</sup>**

MNEMONIC	DIGITAL CODE	$V_{TR-}$	$V_{CODE}$	$V_{TR+}$
-FS	1000	—	-5.000	-4.6875
	1001	-4.6875	-4.375	-4.0625
	1010	-4.0625	-3.750	-3.4375
	1011	-3.4375	-3.125	-2.1825
1/2 -FS	1100	-2.1825	-2.500	-2.1875
	1101	-2.1875	-1.875	-1.5625
	1110	-1.5625	-1.250	-0.9375
BPZ - $1V_{LSB}$	1111	-0.9375	-0.625	-0.3125
BPZ	0000	-0.3125	0.000	+0.3125
BPZ + $1V_{LSB}$	0001	+0.3125	+0.625	+0.9375
	0010	+0.9375	+1.250	+1.5625
	0011	+1.5625	+1.875	+2.1875
1/2 +FS	0100	+2.1875	+2.500	+2.8125
	0101	+2.8125	+3.125	+3.4375
	0110	+3.4375	+3.750	+4.0625
+FS	0111	+4.0625	+4.375	—

(1) Also known as Two's Complement. For this 4-bit system, FSR =  $\pm 5V$ .

(2)  $V_{TR-}$  = lower code transition voltage;  $V_{TR+}$  = upper code transition voltage;  $V_{CODE} = (\text{digital code})_{10} \times V_{LSB}$ ;  $V_{TR+} = V_{CODE} + (1/2)V_{LSB}$ ;  $V_{TR-} = V_{CODE} - (1/2)V_{LSB}$ .

**Bipolar Offset Binary Code (BOB):** BOB coding begins with digital zero (0000, for a 4-bit system) at the negative full-scale. By incrementing the digital count, the corresponding analog value approaches the positive full-scale in  $1V$ , least significant bit (LSB) steps, passing through bipolar zero on the way. This *zero crossing* occurs at a digital code of 1000 (see [Table 2](#)). The digital count continues to increase proportionally to the analog input until the positive full-scale is reached at a full digital count (1111, for a 4-bit system) as seen in [Table 2](#). With BOB coding, the MSB can be considered a sign indicator, whereas a logic '0' indicates a negative analog value, and a logic '1' indicates an analog value greater than or equal to Bipolar Zero (BPZ).

**Table 2. BOB Coding Scheme<sup>(1)(2)</sup>**

MNEMONIC	DIGITAL CODE	$V_{TR-}$	$V_{CODE}$	$V_{TR+}$
-FS	0000	—	-5.000	-4.6875
	0001	-4.6875	-4.375	-4.0625
	0010	-4.0625	-3.750	-3.4375
	0011	-3.4375	-3.125	-2.1825
1/2 -FS	0100	-2.1825	-2.500	-2.1875
	0101	-2.1875	-1.875	-1.5625
	0110	-1.5625	-1.250	-0.9375
BPZ - $1V_{LSB}$	0111	-0.9375	-0.625	-0.3125
BPZ	1000	-0.3125	0.000	+0.3125
BPZ + $1V_{LSB}$	1001	+0.3125	+0.625	+0.9375
	1010	+0.9375	+1.250	+1.5625
	1011	+1.5625	+1.875	+2.1875
1/2 +FS	1100	+2.1875	+2.500	+2.8125
	1101	+2.8125	+3.125	+3.4375
	1110	+3.4375	+3.750	+4.0625
+FS	1111	+4.0625	+4.375	—

(1) FSR =  $\pm 5V$ .

(2)  $V_{TR-}$  = lower code transition voltage;  $V_{TR+}$  = upper code transition voltage;  $V_{CODE} = (\text{digital code})_{10} \times V_{LSB}$ ;  $V_{TR+} = V_{CODE} + (1/2)V_{LSB}$ ;  $V_{TR-} = V_{CODE} - (1/2)V_{LSB}$ .

**Calibration:**

- **Background Calibration–**

Background calibrations are pre-programmed and occur at a scheduled frequency during converter operation without further instructions. During a background calibration, the converter is disconnected from the input signal and an internal offset and/or gain calibration occurs. The results for each calibration are stored in the internal registers of the converter and applied to every conversion after the calibration occurs. The converter algorithm subsequently adds or subtracts the offset calibration value with every conversion result. The converter algorithm also divides the gain calibration value with every conversion.

- **Self-Calibration–**

On command, a self-calibration occurs as the converter is disconnected from the input signal. Once this calibration occurs, the converter performs an internal offset and/or gain calibration algorithm. The converter algorithm subsequently adds or subtracts the offset calibration value with every conversion result. The converter algorithm also divides the gain calibration value with every conversion.

- **System Calibration–**

On command, a system calibration occurs with the input signal connected. In this mode, the converter calibrates offset and gain, including the external input signal(s), on two separate commands. The offset calibration is performed with the assumed zero applied to the input of the converter. The converter algorithm subsequently adds or subtracts the offset calibration value with every following conversion result. The user can then perform the gain calibration with an assumed *full-scale* signal applied to the input. The converter algorithm also divides the gain calibration value with every following conversion.

**Clock:**

- **Duty Cycle–**

The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage value. The duty cycle of a perfect square wave or a differential sine wave is 50%.

- **Jitter–**

The standard deviation of clocking the A/D converter sampling edge (can be a rising edge or falling edge, depending on the specific A/D converter) variation from pulse-to-pulse in time. This instability of the clock signal may cause converter errors as well as an increase in converter noise.

The total jitter includes both aperture and clock jitter, and is equal to:

$$t_j = \sqrt{(t_a^2 + t_c^2)}$$

Where:

- $t_a$  is the root-mean-square of the aperture jitter;
- $t_c$  is the root-mean-square of the clock jitter

There is no correlation between the clock-jitter and aperture-jitter terms; therefore, these terms can be combined on a root-sum-square basis (rss). In most cases, the clock jitter is several times higher than the A/D converter aperture jitter, making the clock jitter the dominant jitter noise source in the system.

Clock jitter can impact the SNR of the converter at medium and higher frequencies. The aperture jitter, along with clock jitter of the sampling system, impacts the overall SNR of the conversion. The contribution of jitter to the SNR of the conversion is equal to:

$$\text{SNR} = 20\log_{10}\left(\frac{1}{(2\pi f t_j)}\right)$$

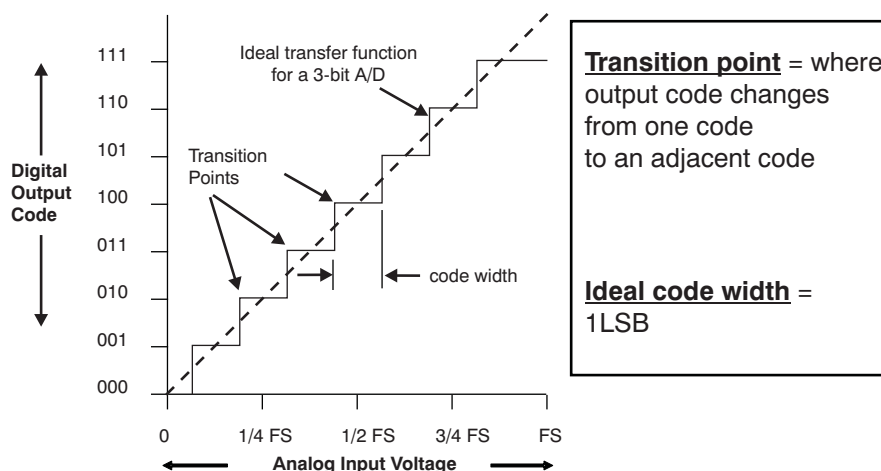
Where:

- $t_j$  is the clock and aperture jitter;
- $f$  is the clock frequency of the converter

- **Slew Rate–**

The time derivative ( $\delta V/\delta t$ ) of the clock signal (digital input or digital output) as it passes through the logic, voltage threshold.

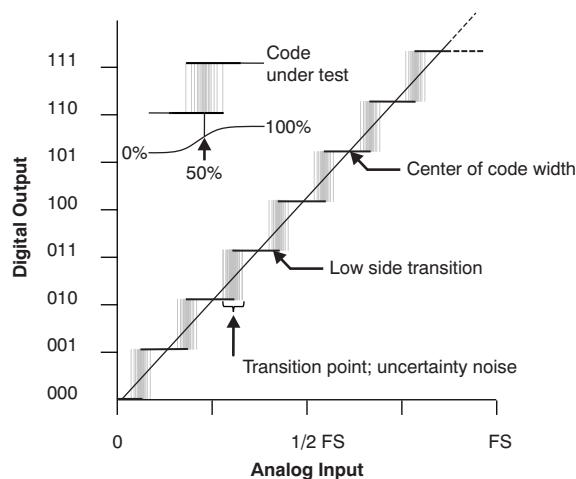
**Code Width:** The code width is the voltage differential between two adjacent transition points of an A/D converter digital output code. The code width is ideally equal to 1LSB. See [Figure 6](#).



NOTE: The unipolar ideal transfer function has zero Offset Error, zero Gain Error, zero DNL error, and zero INL error. In this graph, FS means Full-Scale.

**Figure 6. Unipolar Ideal Transfer Function**

**Code Transition Point (Uncertainty):** The Code Transition Point is the point at which the digital output switches from one code to the next as a result of a changing analog input voltage. The uncertainty or variation in the transition point is a result of internal converter noise, as [Figure 7](#) illustrates.



**Figure 7. A/D Converter Transition Noise**

**Coherent sampling:** Coherent sampling exists when the sampling frequency times the integer number of cycles of the waveform in the data record equals the frequency of the waveform times the number of samples in the data record, where the waveform is periodic. In other words, coherent sampling exists when the following relationship is met:

$$f_s \cdot K = f_t \cdot N$$

Where:

- $f_s$  = the sampling frequency
- $K$  = number of cycles of a waveform in the data record (integer)
- $f_t$  = the waveform frequency
- $N$  = number of samples in the data record



**Complementary Offset Binary (COB):** COB coding begins with digital zero (0000, for a 4-bit system) at the positive full-scale. By incrementing the digital count, the corresponding analog value approaches the negative full-scale in  $-1\text{LSB}$  steps, passing through BPZ on the way. This *zero crossing* occurs at a digital code of 0111 (see Table 3). As the digital count continues to increase, the analog signal goes more negative until the negative full-scale is reached at a full digital count (1111), as shown in Table 3.

With COB coding, like BOB coding, the MSB can also be considered a sign indicator where a logic '1' indicates a negative analog value, and a logic '0' indicates an analog value greater than or equal to BPZ. See Table 3.

**Table 3. COB Coding Scheme<sup>(1)(2)</sup>**

MNEMONIC	DIGITAL CODE	$V_{TR-}$	$V_{CODE}$	$V_{TR+}$
-FS	1111	—	-5.000	-4.6875
	1110	-4.6875	-4.375	-4.0625
	1101	-4.0625	-3.750	-3.4375
	1100	-3.4375	-3.125	-2.1825
1/2 -FS	1011	-2.1825	-2.500	-2.1875
	1010	-2.1875	-1.875	-1.5625
	1001	-1.5625	-1.250	-0.9375
BPZ - $1V_{LSB}$	1000	-0.9375	-0.625	-0.3125
BPZ	0111	-0.3125	0.000	+0.3125
BPZ + $1V_{LSB}$	0110	+0.3125	+0.625	+0.9375
	0101	+0.9375	+1.250	+1.5625
	0100	+1.5625	+1.875	+2.1875
1/2 +FS	0011	+2.1875	+2.500	+2.8125
	0010	+2.8125	+3.125	+3.4375
	0001	+3.4375	+3.750	+4.0625
+FS	0000	+4.0625	+4.375	—

(1) FSR =  $\pm 5V$ .

(2)  $V_{TR-}$  = lower code transition voltage;  $V_{TR+}$  = upper code transition voltage;  $V_{CODE} = (\text{digital code})_{10} \times V_{LSB}$ ;  $V_{TR+} = V_{CODE} + (1/2)V_{LSB}$ ;  $V_{TR-} = V_{CODE} - (1/2)V_{LSB}$ .



**Complementary Straight Binary Code (CSB):** The Complementary Straight Binary coding scheme is the exact digital opposite (that is, one's complement) of *Unipolar Straight Binary*. CSB coding, as with USB code, is also restricted to unipolar systems. When using CSB coding with a digital system, the digital count begins at all zeros (0000, for a 4-bit system) at the positive full-scale value. As the digital code increments, the analog voltage decreases one  $V_{LSB}$  at a time, until 0V is reached at a digital code of 1111. The relationship between CSB coding and its corresponding analog voltages can be seen in [Table 4](#). (In [Table 4](#), BPZ is analogous to Bipolar Zero.)

**Table 4. CSB Coding Scheme<sup>(1)(2)</sup>**

MNEMONIC	DIGITAL CODE	$V_{TR-}$	$V_{CODE}$	$V_{TR+}$
Zero	1111	—	0.000	0.3125
+1 $V_{LSB}$	1110	0.3125	0.625	0.9375
	1101	0.9375	1.250	1.5625
	1100	1.5625	1.875	2.1875
1/4 FSR	1011	2.1875	2.500	2.8125
	1010	2.8125	3.125	3.4375
	1001	3.4375	3.750	4.0625
	1000	4.0625	4.375	4.6875
1/2 FSR	0111	4.6875	5.000	5.3125
	0110	5.3125	5.625	5.9375
	0101	5.9375	6.250	6.5625
	0100	6.5625	6.875	7.1875
3/4 FSR	0011	7.1875	7.500	7.8125
	0010	7.8125	8.125	8.4375
	0001	8.4375	8.750	9.0625
+FS	0000	9.0625	9.375	—

(1) FSR = 10V.

(2)  $V_{TR-}$  = lower code transition voltage;  $V_{TR+}$  = upper code transition voltage;  $V_{CODE} = (\text{digital code})_{10} \times V_{LSB}$ ;  $V_{TR+} = V_{CODE} + (1/2)V_{LSB}$ ;  $V_{TR-} = V_{CODE} - (1/2)V_{LSB}$ .

**Common-mode, DC:**

- **Error–**

Common-mode error is the change in output code when the two differential inputs are changed by an equal amount. This specification applies where a converter has a differential input,  $A_{IN+}$  and  $A_{IN-}$ . This term is usually specified in LSBs.

- **Range–**

The common-mode, analog voltage range at the differential input of the A/D converter while the converter still converts accurate code in accordance with the specific device limits. This specification applies when the input voltages applied to the converters has a relatively small differential input,  $A_{IN+}$  and  $A_{IN-}$ .

- **Signal–**

The input common-mode signal is equal to  $(A_{IN+} + A_{IN-}) / 2$ . Another name for this specification is *Common-mode Voltage*. This specification applies when the input voltages applied to a converter have a differential input,  $A_{IN+}$  and  $A_{IN-}$ .

- **Voltage–**

The common-mode voltage is equal to the sum of the two analog input voltages divided by two.

**Common-mode Rejection Ratio (CMRR):** The Common-mode Rejection Ratio is the degree of rejection of a common-mode signal (dc or ac) across the differential input stage. This specification is the ratio of the resulting digital output signal to a changing input common-mode signal.

**Complementary Twos Complement (CTC):** With CTC coding, digital zero is at an analog voltage that is slightly less (1LSB) than analog bipolar zero. As the digital count increments, the analog voltage becomes more negative until all of the bits are high except for the MSB (0111, for a 4-bit system). At this point, the digital code corresponds to the analog negative full-scale. The next step in incrementing the digital code would be to have the MSB set to a logic '1', and the rest of the bits as logic '0's (1000); this code then represents the analog positive full-scale value. As the digital codes continue to increment, the corresponding analog voltage decreases until BPZ is obtained. Table 5 illustrates this analog/digital relationship. With Complementary Two's Complement coding, the MSB is also a sign indicator with its states of '0' and '1' representing negative and positive voltages, respectively.

**Table 5. CTC Coding Scheme<sup>(1)(2)</sup>**

MNEMONIC	DIGITAL CODE	$V_{TR-}$	$V_{CODE}$	$V_{TR+}$
–FS	0111	—	–5.000	–4.6875
	0110	–4.6875	–4.375	–4.0625
	0101	–4.0625	–3.750	–3.4375
	0100	–3.4375	–3.125	–2.1825
1/2 –FS	0011	–2.1825	–2.500	–2.1875
	0010	–2.1875	–1.875	–1.5625
	0001	–1.5625	–1.250	–0.9375
BPZ – $1V_{LSB}$	0000	–0.9375	–0.625	–0.3125
BPZ	1111	–0.3125	0.000	+0.3125
BPZ + $1V_{LSB}$	1110	+0.3125	+0.625	+0.9375
	1101	+0.9375	+1.250	+1.5625
	1100	+1.5625	+1.875	+2.1875
1/2 +FS	1011	+2.1875	+2.500	+2.8125
	1010	+2.8125	+3.125	+3.4375
	1001	+3.4375	+3.750	+4.0625
+FS	1000	+4.0625	+4.375	—

(1)  $FSR = \pm 5V$ .

(2)  $V_{TR-}$  = lower code transition voltage;  $V_{TR+}$  = upper code transition voltage;  $V_{CODE} = (\text{digital code})_{10} \times V_{LSB}$ ;  $V_{TR+} = V_{CODE} + (1/2)V_{LSB}$ ;  $V_{TR-} = V_{CODE} - (1/2)V_{LSB}$ .

**Conversion Cycle:** A conversion cycle is a discrete A/D converter operation, and refers to the process of changing the input signal to a digital result. When performed by a SAR converter, for example, the conversion occurs after the sample is acquired. For delta-sigma converters, a conversion cycle refers to the  $t_{\text{DATA}}$  time period (that is, the period between each data output). With delta-sigma converters, each digital output is actually based on the modulator results from several  $t_{\text{DATA}}$  time periods.

**Conversion Maximum Rate:** The maximum sampling rate of a device while performing within specified operating limits. All parametric testing is performed at this sampling rate unless otherwise noted. (Also see [Sample Rate](#).)

**Conversion Minimum Rate:** The minimum conversion rate is the minimum sampling rate at which the A/D converter meets its stated specifications.

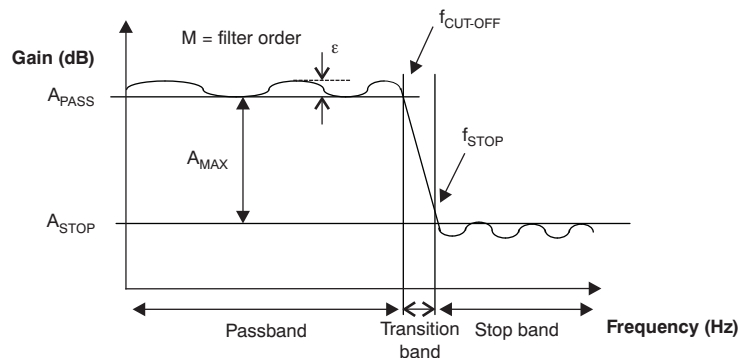
**Conversion Rate:** The frequency of the digital output words at the output of the converter. (See also [Sample Rate](#).)

**Conversion Speed:** See [Sample Rate](#).

**Conversion Time:** After sampling the signal, the conversion time is the time required for a SAR or pipeline A/D converter to complete a single conversion. The conversion time does not include the acquisition time or multiplexer set-up time. The conversion time for a given device is less than the throughput time.

**Crosstalk:** This term refers the condition in which a signal affects another nearby signal. With A/D converters, this event is the occurrence of an undesirable signal coupling across a multi-channel A/D converter from one channel that is not being used in the conversion to another channel that is part of the signal path. This undesired coupling is a result of capacitive or conductive coupling from one channel to another. This interference appears as noise in the output digital code.

**Cutoff Frequency:** The cutoff frequency ( $f_{\text{CUT-OFF}}$ ) of a low-pass analog or digital filter is commonly defined as the  $-3\text{dB}$  point for a Butterworth and Bessel filter, or the frequency at which the filter response leaves the error band for the Chebyshev filter. See [Figure 8](#).



**Figure 8. Key Analog and Digital Filter Design Parameters**

**Data Rate or Data Output Rate:** The rate at which conversion results are available from a converter. For a SAR converter, the data rate is equal to the sampling frequency,  $f_s$ . With a delta-sigma converter, the data rate is equal to the modulator frequency ( $f_{\text{MOD}}$ ) divided by the decimation ratio.

**Data Valid Time:** The time (as measured in A/D converter clock cycles) between the first clock transition where data is valid and the last clock transition where data is no longer valid.

**Decibels (dB):** Decibels are a logarithmic unit used to describe a ratio of two values; one value is measured while the other value is a reference. The ratio may measure power, sound pressure, voltage, or intensity.

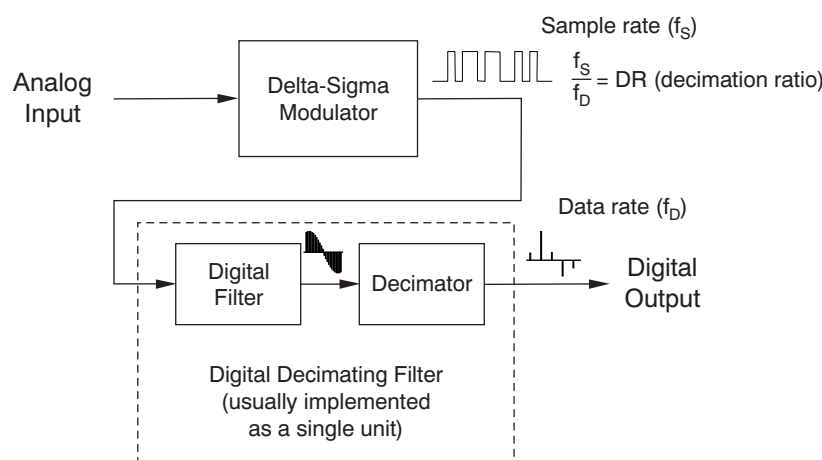
**dBFS:** dBFS is the decibel measurement as it is referred to the full-scale input range.

**dBc:** Decibels referenced to a carrier, or decibels below a carrier. For example, a spurious signal or distortion less than  $-40\text{dBc}$  means that the distortion is at least 40dB less than the specified carrier signal or desired signal level.

**dBm:** dBm represents a measured power level in decibels relative to 1mV.

**Decimation Ratio:** The decimation ratio is the ratio between the output sampling rate of the delta-sigma modulator and the output data rate of a delta-sigma converter as performed by the decimator. The decimator is a block that decimates or discards some results. The decimation ratio sets the number of data samples from the modulator that are averaged together to get a result. Higher decimation ratios average a greater number of values together, thereby producing lower noise results.

**Delta-Sigma Converter ( $\Delta\Sigma$ ):** A delta-sigma converter is a one-bit (or multi-bit) sampling system (see [Figure 9](#)). In this system, multiple bits are sent serially through a digital filter where mathematical manipulation is performed. This diagram illustrates a FIR (Finite Impulse Response) filter. Another filter option could be IIR (Infinite Impulse Response). Also see [Digital Filter](#).



NOTE: The analog portion of a delta-sigma converter can be modeled using an optional input Programmable Gain Amplifier (PGA), followed by a charge-balancing A/D converter. The digital portion is modeled using a low-pass digital filter followed by a digital decimation filter.

**Figure 9. Block Diagram of a Delta-Sigma A/D Converter**

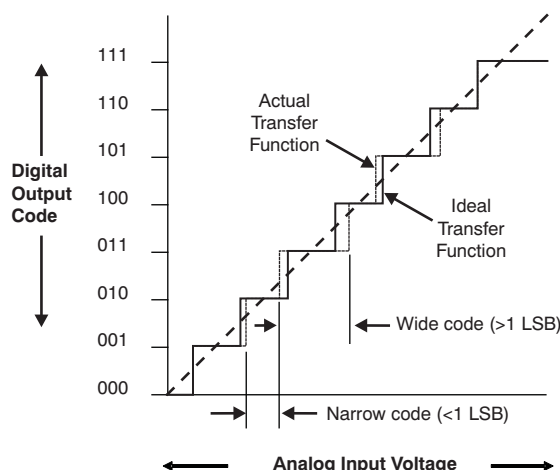
**Differential Gain:** see [Gain](#).

**Differential Gain Error:** see [Gain Error](#).

**Differential Phase Error:** The difference in phase between a reconstructed output and a small-signal input.

**Differential Nonlinearity (DNL):** An ideal A/D converter exhibits code transitions at analog input values spaced exactly 1LSB apart ( $1\text{LSB} = V_{\text{FS}} / 2^n$ ). DNL is the deviation in code width from the ideal 1LSB code width. A DNL error less than  $-1\text{LSB}$  can cause missing codes.

DNL is a critical specification for image-processing, closed-loop, and video applications. This is a *dc* specification, where measurements are taken with near-dc analog input voltages. Other *dc* specifications include [Offset Error](#), [Gain Error](#), [INL](#), [Total Unadjusted Error \(TUE\)](#), and [Transition Noise](#). [Figure 10](#) illustrates the ideal transfer function as a solid line and the DNL error as a dashed line.



NOTE: DNL is the difference between an ideal code width and the measured code width.

**Figure 10. Differential Nonlinearity Error**

**Digital Filter:** A digital filter uses on-chip digital functions to perform numerical calculations on sampled values of the input signal. The on-chip digital functions are dedicated functions included in the delta-sigma converter. A digital filter works by performing digital math operations on an intermediate form of the signal. This process contrasts with that of an analog filter, which works entirely in the analog realm and must rely on a physical network of electronic components (such as resistors, capacitors, transistors, etc.) to achieve a desired filtering effect.

**Digital Filter, Finite Impulse Response (FIR) filter:** A finite impulse response (FIR) filter is a type of a digital filter. It is *finite* because its response to an impulse ultimately settles to zero. This type of response contrasts with an infinite impulse response (IIR) filter that has internal feedback and may continue to respond indefinitely. An FIR filter has a number of useful properties. FIR filters are inherently stable. This stability exists because all the poles are located at the origin and are therefore located within the unit circle. The FIR filter is a linear-phase or linear-plus-90°-phase response digital filter. A moving average filter is a very simple FIR filter.

**Digital Filter, Infinite Impulse Response (IIR) filter:** IIR filters have an impulse response function that is non-zero over an infinite length of time. This characteristic contrasts with finite impulse response filters (FIR), which have fixed-duration impulse responses. Analog filters can be effectively realized with IIR filters.

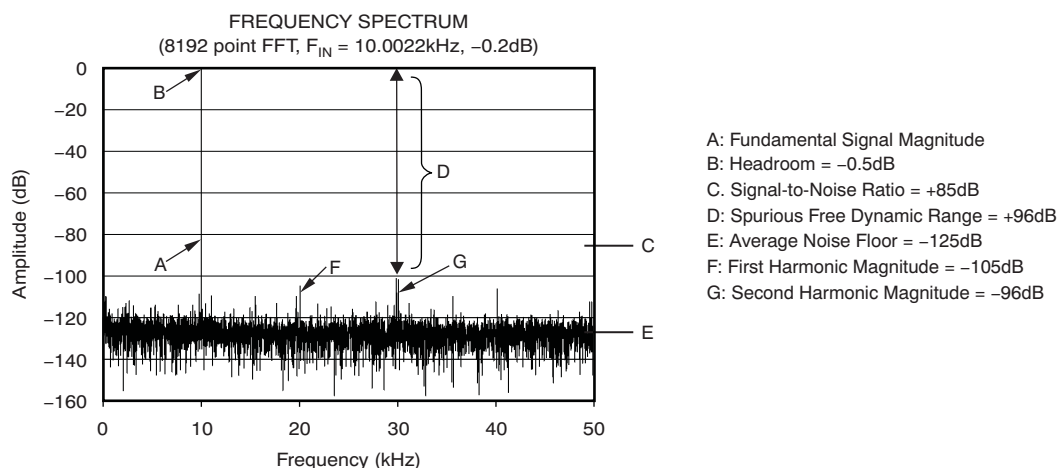
**Digital Interface, SPI™:** – Serial peripheral interface, or SPI, is a three- or four-wire interface. With this interface, the A/D converter is typically a slave device. A/D converters with SPI capability communicate using a master/slave relationship, in which the master initiates the data frame. When the master generates a clock and selects a slave device, the data is either transferred in or out, or in both directions simultaneously.

SPI specifies four signals: clock (SCLK); master data output, slave data input (MOSI); master data input, slave data output (MISO); and slave select (SS). SCLK is generated by the master and input to all slaves. MOSI carries data from master to slave. MISO carries data from slave back to master. A slave device is selected when the master asserts its  $\overline{CS}$  signal. Because it lacks built-in device addressing, SPI requires more effort and more hardware resources than I<sup>2</sup>C™ when more than one slave is involved, but SPI tends to be more efficient and straightforward than I<sup>2</sup>C in point-to-point (single master, single slave) applications. SPI can also achieve significantly higher data rates than I<sup>2</sup>C.

**Digital Interface, I<sup>2</sup>C™:** I<sup>2</sup>C is a two-wire (SDA and SCL) Philips standard interface. The I<sup>2</sup>C interface is an 8-bit serial bus with bi-directional data transfer capability. The speeds for I<sup>2</sup>C are 100kbit/s, 400kbit/s and 3.4Mbit/s. Devices connected to the network are addressable, having unique addresses. This interface protocol has collision detection and arbitration to prevent data corruption with two or more masters on line.

**Dynamic Range:** The ratio of the maximum input signal to the smallest input signal. Dynamic range can be specified in terms of SFDR or SNR. This critical specification sets the limits on the detectable maximum and minimum analog signal.

**Dynamic Specifications:** These are product data sheet specifications where the input to the A/D converter is an ac signal. This group of specifications includes: [Signal-to-Noise Rejection \(SNR\)](#), [Signal-to-Noise Ratio plus Distortion \(SINAD or SNR+D\)](#), [Effective Number Of Bits \(ENOB\)](#), [Total Harmonic Distortion \(THD\)](#), [Spurious Free Dynamic Range \(SFDR\)](#), [Intermodulation Distortion \(IMD\)](#), and [Full-power Bandwidth \(FPBW\)](#). See Figure 11.



**Figure 11. Dynamic Specifications (FFT Plot)**

**Effective Number of Bits (ENOB):** ENOB is a critical performance limit with digital oscilloscope/waveform recorders, as well as with image processing, radar, sonar, spectrum analysis, and telecommunications applications. This critical specification often describes the dynamic performance of the A/D converter. See also [Dynamic Specifications](#).

- **Effective Number of Bits vs SINAD—**

The units of measure for signal-to-noise-ratio plus distortion (SINAD) are dB and the units of measure for ENOBs are bits. SINAD is converted into ENOB through this calculation:

$$\text{ENOB} = \frac{(\text{SINAD} - 1.76)}{6.02}$$

- **Effective Number of Bits vs SNR of Delta-Sigma Converters—**

This value defines the usable resolution of the delta-sigma A/D converter in bits. ENOB is determined by applying a fixed, known dc voltage to the analog input and computing the standard deviation from several conversions. Calculate ENOB using data taken from the device. ENOB is equivalent to:

$$\text{ENOB} = n - \log_2(\sigma)$$

where:

- $\sigma$  = standard deviation of data
- $n$  = number of converter bits

If 2.72 bits (the industry standard, with a crest factor = 3.3) is subtracted from bits-rms, the resulting units are peak-to-peak bits. Noise volts peak-to-peak ( $V_{PP}$ ) in a signal is equal to (Noise volts rms \* 2 \* CF). The Noise bits peak-to-peak is equal to (Noise in bits rms – BCF [see [Table 6](#)]). From the selected CF (crest factor), the probability of an occurrence that exceeds defined peak-to-peak limits is predicted.

[Table 6](#) summarizes the relationship between crest factor, subtracted bits from RMS bits, and the percentage of noise events outside the peak defined.

**Table 6. Relationship Between Crest Factor, Digital Crest Factor, and Probability of Occurrence**

Crest Factor (CF)	Crest Factor in Bits (BCF, bits)	Percentage of Occurrences <sup>(1)</sup>
2.6	–2.38	1%
3.3	–2.72	0.1% (Industry-standard; accepted values)
3.9	–2.94	0.01%
4.4	–3.13	0.001%
4.9	–3.29	0.0001%

<sup>(1)</sup> Percentage of occurrences where peaks are exceeded

**Effective Resolution:** Effective resolution describes the useful bits from an A-D conversion as they relate to the input signal noise, and is equivalent to the effective number of bits ([ENOB](#)). Volts or bits are the units of measure for this specification. This measurement can be confused with the actual resolution that is commonly stated in product data sheet titles. The actual resolution is simply the number of converter bits that are available at the output of the device, without clarifying whether or not these bits are noise-free. Effective resolution is expressed using two different units of measure. The specification of *bits rms* refers to output data. This specification predicts the probability of a conversion level of repeatability of 70.1% for a dc input signal. *Volts rms* ( $V_{RMS}$  or  $V_{rms}$ ) refers to the input voltage. Also see [Effective Number of Bits](#).

**Effective Resolution Bandwidth:** The effective resolution bandwidth is the highest input frequency where the SNR is dropped by 3dB for a full-scale input amplitude.

**Fall Time:** The time required for a signal to fall from 90% of the transition range to 10% of that range.

**Fourth Harmonic (HD4):** The fourth harmonic is four times the frequency of the fundamental.

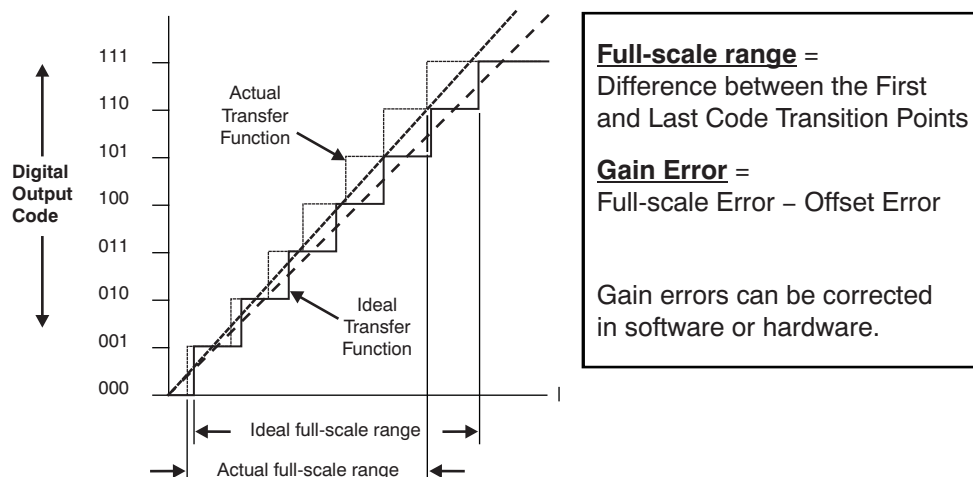
**Full-power Bandwidth (FPBW):** The frequency where the reconstructed output of the A/D converter is 3dB below the full-scale value of a full-scale input signal. Other dynamic or ac specifications include the [Signal-to-Noise Ratio \(SNR\)](#), [Signal-to-Noise Ratio plus Distortion \(SINAD or SNR+D\)](#), [Effective Number Of Bits \(ENOB\)](#), [Total Harmonic Distortion \(THD\)](#), [Spurious Free Dynamic Range \(SFDR\)](#), and [Intermodulation Distortion \(IMD\)](#); see also [Dynamic Specifications](#).

**Full-scale (FS or FSR):** See [Analog Input, Voltage Range, Full-Scale \(FS or FSR\)](#).

**Gain:** Gain is a value at which the input values are multiplied with the offset error removed.

**Gain Error (Full-Scale Error):** Gain error is the difference between the ideal slope between zero and full-scale (as well as negative full-scale for differential input A/D converters) and the actual slope between the measured zero point and full-scale. Offset errors are zeroed out for this error calculation. This is a dc specification, using a near-dc analog input voltage for measurements. Other critical dc specifications include [Offset Error](#), [DNL](#), [INL](#), and [transition noise](#). See [Figure 12](#).





NOTE: Gain error is the difference between the ideal gain curve (solid line) and the actual gain curve (dashed line) with offset removed.

**Figure 12. Gain Error**

**Gain Temperature Drift:** Gain temperature drift specifies the change from the gain value at the nominal temperature to the value at  $T_{MIN}$  to  $T_{MAX}$ . It is computed as the maximum variation of gain over the entire temperature range divided by  $(T_{MAX} - T_{MIN})$ . The units of measure for this specification is parts per million per degree C (ppm /°C).

**Group Delay:** Group delay is the rate of change of the total phase shift with respect to angular frequency or  $\delta\Phi/\delta\omega$ , where  $\Phi$  is the total phase shift in radians, and  $\omega$  is the angular frequency in radians per unit time ( $\omega$  equal to  $2\pi f$ ), where  $f$  is the frequency (hertz if group delay is measured in seconds). With delta-sigma converters, the group delay is caused by the digital filters.

**Harmonic Distortion:** The ratio of the rms input signal to the rms value of the harmonic in question. Typically, the magnitude of the input signal is 0.5dB to 1dB below full-scale in order to avoid clipping. When the input signal is much lower than full-scale, other distortion entities may limit the distortion performance as a result of the converter DNL. When determining the ac linearity of a device, harmonic distortion is used when a single tone is applied. Harmonic distortion can be specified with respect to the full-scale input range (dBFS or dB), or with respect to the actual input signal amplitude (dBc). (Also see [second harmonic - HD2](#), [third harmonic - HD3](#), and [fourth harmonic - HD4](#).)

**I<sup>2</sup>C Interface** See [Digital Interface](#), I<sup>2</sup>C.

**Ideal Code Width (q):** The ideal full-scale input voltage range divided by the total number of code bins. The total number of code bins equals:

$$q = \frac{FS}{2^n}$$

Where:

- total number of code bins =  $2^n$ ;
- $n$  = number of bits;
- FS = Full-Scale Range

**Ideal A/D Converter Transfer Function:** An analog voltage is mapped into  $n$ -bit digital values with no offset, gain, or linearity errors. See [Figure 6](#).

**Idle Tones:** These tones are caused by the interaction between the delta-sigma A/D converter modulator and digital filter. Idle tones come from two sources. One is inherent in the voltage being measured, such as when the modulator output repeats in a pattern that cannot be filtered by the digital filter. This type of

pattern occurs at 0V, one-half the FSR, three-fourths of the FSR, etc. The second source of idle tones is the chopping frequency being sampled in to the measurement. This sampled frequency produces a digital pattern of codes that *oscillate* at a slow frequency within the passband. As the name implies, idle tones can appear as a frequency in the output conversion data with multiple dc input conversions at a constant data rate. Patented techniques are available to reduce idle tone concerns.

**Input range (FS or FSR):** The specified range of the peak-to-peak, input signal of an A/D converter.

**Integral Nonlinearity (INL, also known as Relative Accuracy Error):** An INL error is the maximum deviation of a transition point from the corresponding point of the ideal transfer curve, with the measured offset and gain errors zeroed. This specification can be referenced to a best-fit transfer function or an end-point transfer function. The best-fit INL results will be one-half the error of the end-point measurement method for the same device. The best-fit transfer function is determined with a least squares curve fit to the transfer function. This is a *dc* specification, where measurements are taken with near-dc analog input voltages. The units for INL are LSB. INL is a critical specification for image processing applications. Other critical dc specifications include [Offset Error](#), [Gain](#), [TUE](#), [DNL](#), and [transition noise](#). See [Figure 13](#).

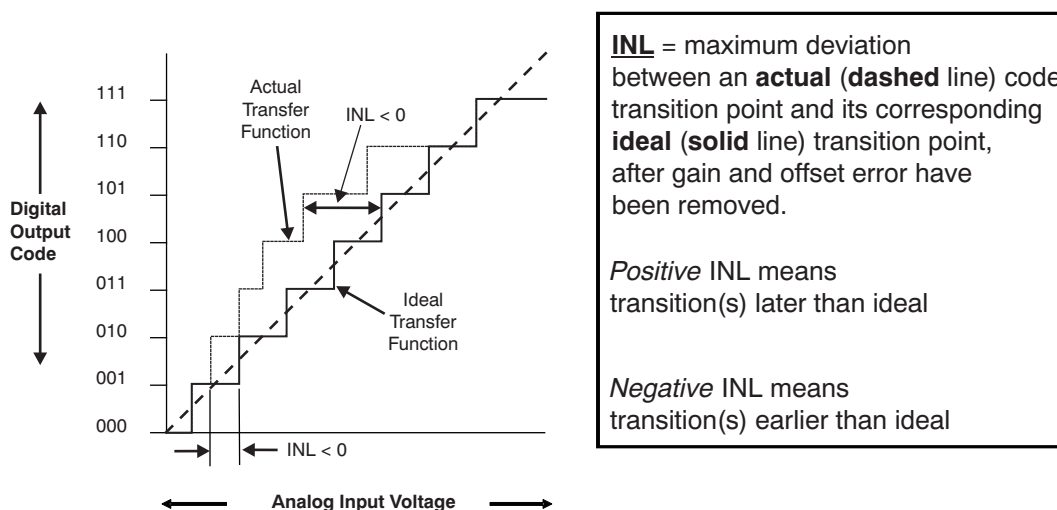


Figure 13. Integral Nonlinearity Error

**Intermodulation Distortion (IMD):** The A/D converter can create additional spectral components as a result of the input of two sinusoidal frequencies simultaneously applied at the input. IMD is the ratio of power of the intermodulation products to the total power of the original frequencies. IMD is either given in units of dBc (when the absolute power of the fundamental is used as the reference) or dBFS (when the power of the fundamental is extrapolated to the converter full-scale range).

Two-tone intermodulation distortion, or IMD3, is the ratio of the power of the fundamental (at frequencies  $f_1$  and  $f_2$ ) to the power of the worst spectral component at either frequency ( $2f_1 - f_2$  or  $2f_2 - f_1$ ). IMD3 is given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or in units of dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

IMD is a critical specification for radar, sonar, spread spectrum communication, telecommunication, and wideband digital receiver applications. Other dynamic or ac specifications include the [Signal-to-Noise Ratio \(SNR\)](#), [Signal-to-Noise Ratio plus Distortion \(SINAD or SNR+D\)](#), [Effective Number Of Bits \(ENOB\)](#), [Total Harmonic Distortion \(THD\)](#), [Spurious Free Dynamic Range \(SFDR\)](#), and [Full-power Bandwidth \(FPBW\)](#).

**Internal Buffer:** If the A/D converter has an input buffer at its input, this provides a high impedance input that *isolates* the external input signal from the sampling effects of the converter and provides a higher input impedance.

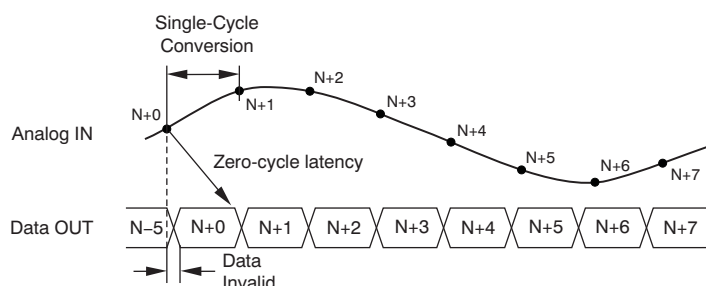
**Jitter:** see [Aperture Jitter](#) and [Clock Jitter](#).

**Large Signal:** A large signal is where the peak-to-peak amplitude of a signal spans at least 90% of the full-scale analog range of an A/D converter.

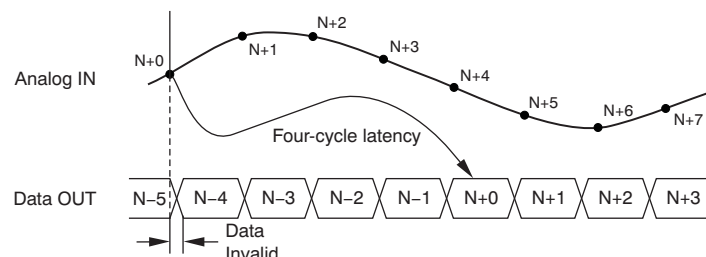
## Latency:

**Cycle latency:** For A/D converters, cycle-latency is equal to the number of complete data cycles between the initiation of the input-signal conversion and the initiation of the next signal conversion. The unit of measure for this definition of latency is *(n)-cycle latency*, where *n* is a whole number. Figure 14 illustrates the cycle-latency behavior of two different A/D converters. Figure 14A shows a timing diagram for a zero-cycle latency A/D converter; Figure 14B shows a timing diagram for a four-cycle latency A/D converter. An A/D converter with zero-cycle latency can also be described as having *single-cycle settling* or *single-cycle conversion*.

A. Zero-cycle Latency



B. Four-cycle Latency



NOTE: With zero-cycle latency (A), the sampling period of N+0 is initiated. The output data of N+0 are acquired before the sampling period of N+1 is initiated. With four-cycle latency (B), the sampling period of N+0 is initiated. The output data of N+0 are acquired after four cycles.

**Figure 14. Input/Output Characteristics of an A/D Converter with (A) Zero-Cycle Latency and (B) Four-Cycle Latency**

**Latency-time:** Latency-time is the time required for an ideal step-input to converge, within an error margin, to a final digital output value. This error-band is expressed as a pre-defined percentage of the total output voltage step. The latency-time of a conversion is that period between the time where the signal acquisition begins to the time the next conversion starts. In contrast to the cycle-latency specification, the latency-time (or settling-time) is never equal to zero.

**Latency-Time, Delta-Sigma Converter:** For delta-sigma A/D converters, latency is harder to define because delta-sigma A/D converters do not output a code corresponding to a single point in time. The code that  $\Delta\Sigma$  converters output is the result of filtering or averaging the input during an interval of time; the interval is equal to the sample period. For this reason, we measure latency for a delta-sigma A/D converter by starting at the beginning of a sample period, and measuring to the time that data can be retrieved. It may also be practical to include in the latency time the time needed to retrieve the data, since delta-sigma A/D converters nearly always have serial interfaces. For audio converters, this additional latency can be very significant, even up to several tens of sample periods. For low-speed industrial converters with sinc filters, it sometimes amounts to only a few modulator cycles. For delta-sigma A/D converters, filters with constant group delay are almost always used, so there is no difference between group delay and latency. The latency-time of a delta-sigma converter is often called *Settling time*.

**Latency-Time, SAR Converter:** For SAR A/D converters, latency is typically very short; it is the amount of time needed for the successive approximation process to complete. Data is typically available immediately afterward. This approach is typically equal to the conversion time, and exclusive of the sample time. For SARs, which generally have an external continuous-time analog filter at the front-end, group delay can be a more useful measurement, since the latency may be frequency-dependent.

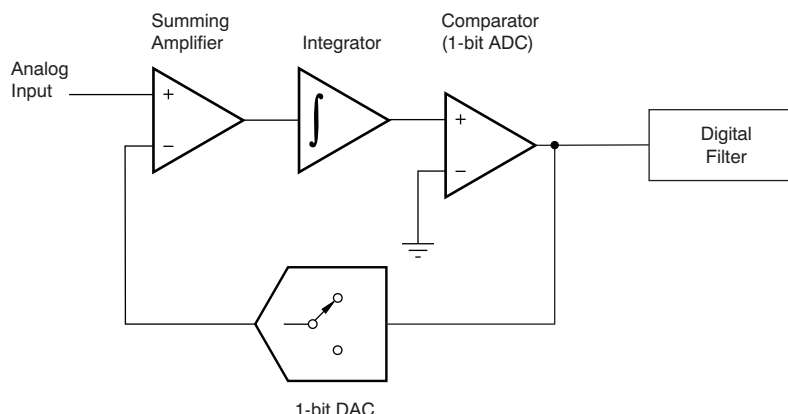
**Latency-Time, Pipeline Converter:** The number of complete clock cycles between the initiation of a conversion and when the data appears on the output driver stage.

**Least Significant Bit (LSB):** The least significant bit is the bit representation of the smallest analog input signal that is converted, and is synonymous with the code bin width. The least significant bit defines the resolution of the converter. It is also referred to the furthest right bit in a binary digital word.

**Major Carry Transition:** The mid-scale point where the MSB changes from low to high and all other bits change from high to low, or where the MSB changes from high to low and all other bits change from low to high. These transition points are often where the worst switching noise occurs. (See also [Most Significant Bit or MSB.](#))

**Missing Code:** A missing code is when a legitimate A/D converter output code that should exist is not available. An increase in the analog voltage can produce an unexpected smaller or the same digital output code. See [Figure 17.](#)

**Modulator:** At the input of a first-order modulator, the signal comes in through a summing amplifier (see [Figure 15](#)). The signal then passes through an integrator that feeds a comparator. The comparator acts like a one-bit quantizer. The output of the comparator feeds forward to a digital filter and back to a one-bit Digital-to-Analog (D/A) Converter. The signal at the inverted output of the D/A converter is summed into the input summer. The output of a modulator provides a stream of digital ones and zeros. The time average of this serial output is proportional to the analog input voltage. The order of the modulator is equivalent to the number of integrators and feedback loops.

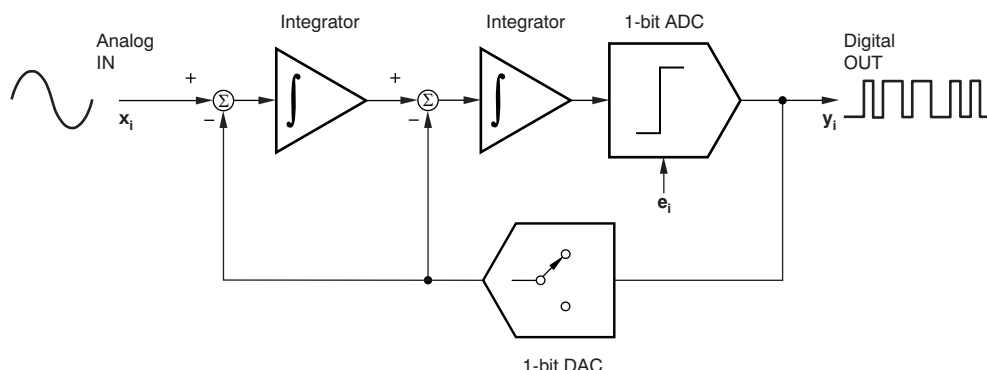


NOTE: For the entire delta-sigma ADC block diagram, refer to [Figure 9.](#)

**Figure 15. First-Order Modulator Segment (Delta-Sigma A/D Converter)**

### Modulator, continued:

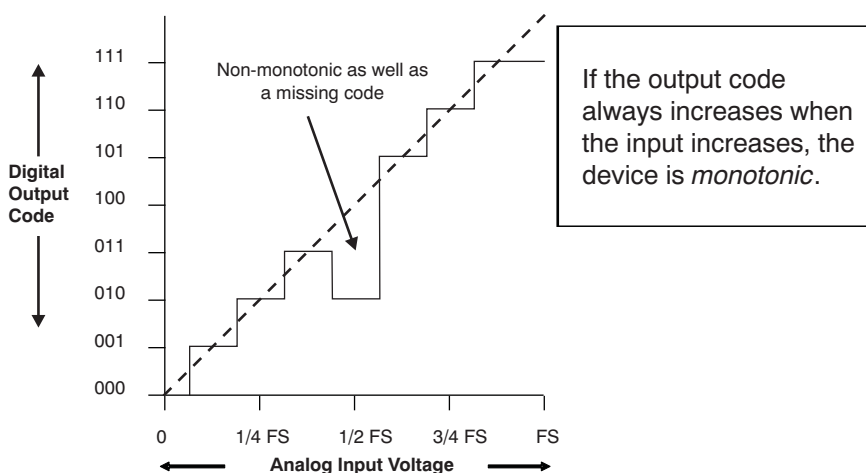
Figure 16 illustrates a second-order modulator. It is not uncommon to have a third-, fourth-, fifth- or sixth-order modulator inside a delta-sigma A/D converter. The number of output bits can also be higher than one. A modulator can be included in a delta-sigma A/D converter chip or it can be a stand-alone component. The combination of a modulator and a processor (programmed to implement a digital filter) results in a high-resolution A/D converter system.



NOTE: For the entire delta-sigma ADC block diagram, refer to Figure 9.

**Figure 16. Second-Order Modulator Segment (Delta-Sigma A/D Converter)**

**Monotonic:** This term implies that an increase (or decrease) in the analog voltage input will always produce no change or an increase (or decrease) in the digital code. Monotonicity does *not* imply there are no missing codes. Monotonicity is a critical specification with automatic control applications. See Figure 17.



NOTE: In this graph, FS means Full-Scale.

**Figure 17. Non-monotonic Transfer Function**

**Most Significant Bit (MSB):** The most significant bit is often considered as the furthest left bit in a binary digital word. The most significant bit can serve as the sign bit in bipolar converters. For more information about the definition of the MSB, refer to [Bipolar Offset Binary Code \(BOB\)](#), [Complementary Offset Binary Code \(COB\)](#), [Complementary Straight Binary Code \(CSB\)](#), [Complementary Twos Complement \(CTC\) Code](#), or [Unipolar Straight Binary Code \(USB\)](#).

**Multiplexer (MUX):** A multiplexer selects one of several input signals into a single output signal. At the input of an A/D converter with a multiplexer, one signal (which can be a single-ended or differential input) is selected from several inputs.

**No Missing Codes:** This term implies that an increase (or decrease) in the analog voltage input will always produce an increase (or decrease) in digital output converter code. A converter with no missing codes is also [monotonic](#) to specified bits. See [Figure 17](#).

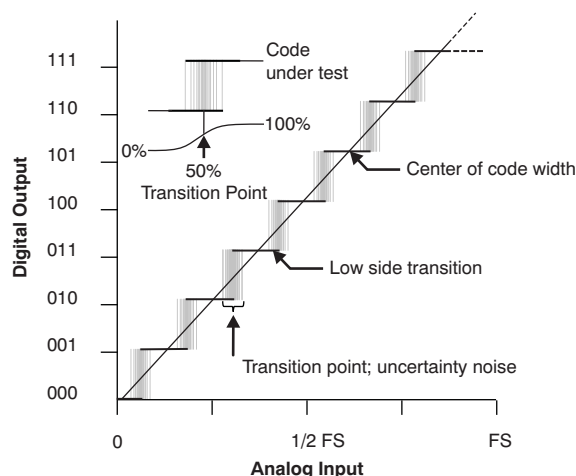
**Noise, A-D Converter:** Any deviation between the output digital code with a dc, noise-free, input analog signal. Examples of noise include random noise, nonlinearities such as harmonic distortion, and aperture uncertainty.

- **Random Noise—**

A random fluctuation in the output code of an A/D converter.

- **Uncertainty Noise—**

The transition point is typically not a single threshold, but rather a small region of uncertainty. The region of uncertainty is defined with repetitive code transitions on a given code. The transition point is the statistical average of these repetitive transitions. This is a *dc* specification. Other *dc* specifications include [Offset Error](#), [Gain](#), [DNL](#), [INL](#), and [TUE](#). See [Figure 18](#). (Also see [Code Transition Point](#).)



NOTE: This non-ideal transfer function of a 3-bit A/D converter illustrates the transition noise of every code. In this graph, FS means Full-Scale.

**Figure 18. Non-Ideal Transfer Function (3-bit A/D Converter)**

**Noise Power Ratio (NPR):** The dynamic performance of an A/D converter with a broad bandwidth input can be characterized by measuring the noise power ratio (NPR). In A/D converter applications where the input signal contains a large number of incoherent tones or narrow bandwidth signals, it is generally desired that distortion (resulting from combinations of strong signal components) should not interfere with detection of weaker signal components. For an A/D converter sample set, NPR is the ratio of the average out-of notch to the average in-notch power spectral density magnitudes. This parameter is a critical specification in spread spectrum communication applications. A/D converters having measured noise power ratios that closely match theoretical NPR, for an ideal *N*-bit device, are desirable candidates for broadband signal applications.

**Normal-mode Rejection (NMR):** Normal-mode rejection is the degree of rejection of a common-mode signal (dc or ac) across the differential input stage. This specification is the ratio of the changing input common-mode signal to the resulting digital output. NMR is the same as CMR; also see [Common-Mode Rejection](#).

**Number of Converter Bits (n):** The number of converter bits ( $n$ ) represents the number of bits in the output digital word. The number of output codes that an A/D converter produces is  $2^n$  possible codes.

**Nyquist Theorem:** When sampling a signal at discrete intervals, this theorem postulates that theoretically, the sampling speed must be greater than twice the bandwidth of the input signal being sampled. The Nyquist frequency is half of the sample rate. When the signal bandwidth is less than half of the sample rate, the original signal can theoretically be reconstructed.

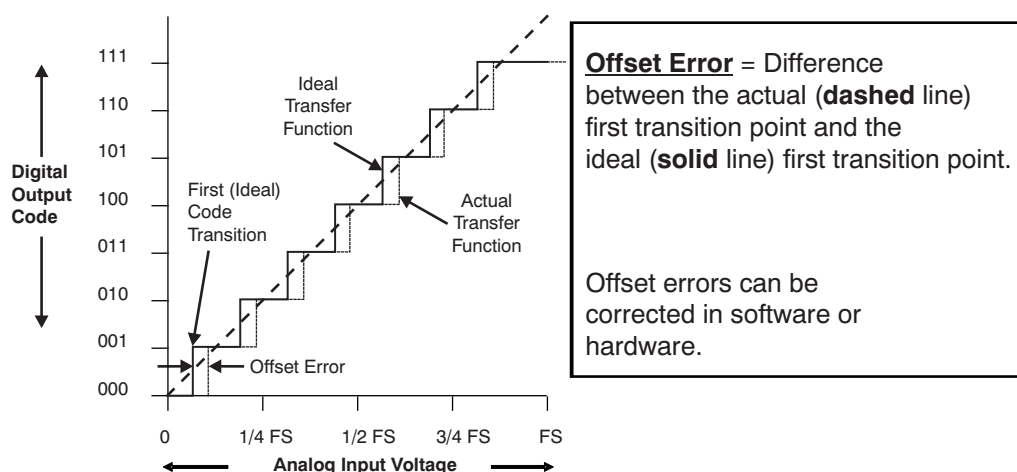
**Offset Error:** Offset error is the difference in voltage between the ideal first code transition and the actual code transition of an A/D converter. This is a dc specification, where measurements are taken with near-dc analog input voltages. Other dc specifications include [Gain](#), [DNL](#), [INL](#), and [Transition Noise](#).

**Offset Error, Unipolar:** In a unipolar device, offset error is the difference between the first measured transition point (lowest in voltage) and the first ideal, transition point. (See [Figure 19](#).) Unipolar Offset Error is measured and calculated as shown in the following equation:

$$\text{Offset Error} = (V[0:1] - (0.5)V_{\text{ILSB}})$$

Where:

- $V_{\text{ILSB}} = V_{\text{REF}} / 2^n = \text{ideal LSB voltage size};$
- $V[0:1] = \text{analog voltage of first transition};$
- $V_{\text{REF}} = \text{full-scale voltage};$
- $n = \text{number of converter bits}$



NOTE: In this graph, FS means Full-Scale.

**Figure 19. Unipolar Offset Error**

**Offset Error, Bipolar:** For a bipolar device, offset error is the deviation of output code from mid-code or mid-scale (or zero) when both inputs are tied to a common-mode voltage.

**Offset Error, Temperature Drift:** Temperature drift specifies the change from the offset value at the nominal temperature to the value at  $T_{\text{MIN}}$  to  $T_{\text{MAX}}$ . It is computed as the maximum variation of offset over the entire temperature range divided by  $(T_{\text{MAX}} - T_{\text{MIN}})$ . The units of measure for this specification are parts per million per degree Celsius (ppm/°C) or microvolts per degree Celsius ( $\mu\text{V}/^\circ\text{C}$ ).

**Output Data Format:** See [Bipolar Offset Binary Code \(BOB\)](#), [Complementary Offset Binary Code \(COB\)](#), [Complementary Straight Binary Code \(CSB\)](#), [Complementary Twos Complement \(CTC\) Code](#), or [Unipolar Straight Binary Code \(USB\)](#).

**Output Hold-time:** The amount of time that the output data of the converter is valid.

**Overrange Recovery** (also known as **out-of-range recovery** or **over voltage recovery**): After the analog input signal goes beyond the absolute input range and returns to the specified input range, the overrange recovery time is the time required for the converter to make conversions at its rated accuracy.

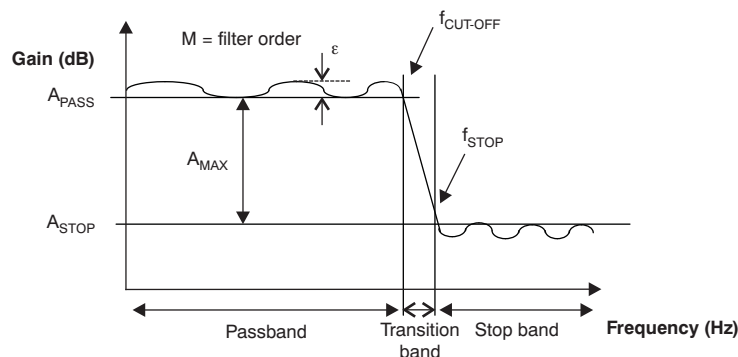


**Oversampling:** With an oversampling converter, the sample rate of the A/D converter is at a much higher frequency than the converted analog frequency bandwidth. The Nyquist frequency  $f_{\text{NYQUIST}}$  is:

$$f_{\text{NYQUIST}} > 2 \times f_{\text{SIGNAL}}$$

where  $f_{\text{SIGNAL}}$  is the highest frequency of interest in the input signal. The advantages of oversampling are the lowering of the quantization noise contained within the passband, and moving harmonics out of the band of interest. Increasing the Oversampling Rate by two theoretically improves SNR by 3dB. Using Oversampling techniques makes anti-aliasing filter design easier. (Also see [Nyquist Theorem](#).)

**Passband:** With an analog filter, the frequency span from dc to the analog cutoff frequency is defined as the *passband region*. The magnitude of the response in the passband is defined as  $A_{\text{PASS}}$ , as shown in [Figure 20](#). The response in the passband can be flat, with no ripple, as it is when an analog Butterworth or Bessel filter is designed. Conversely, a Chebyshev filter has a ripple up to the cutoff frequency. The magnitude of the ripple error of a filter is defined as  $\epsilon$ .



**Figure 20. Key Analog Filter Design Parameters**

**Parallel Interface:** A parallel interface is where the A/D converter interface is capable of transferring more than one bit simultaneously. The other type of A/D converter interface is a serial interface.

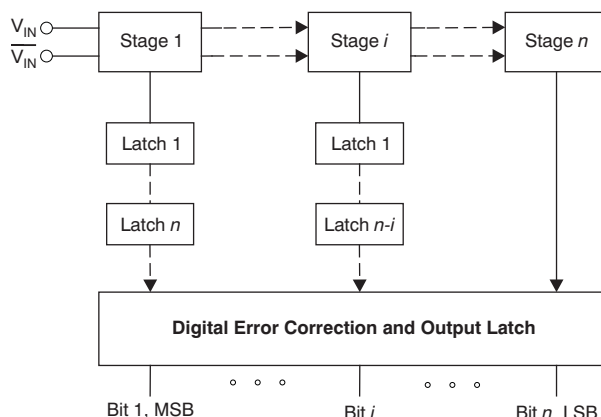
**Phase Noise:** Phase noise describes short-term, random frequency fluctuations (or time-based jitter) of a clock or input signal. Frequency stability is a measure of the degree to which an oscillator maintains the same value of frequency over a given time. When phase noise is measured, it shows small variations in the frequency phase angle with the signal magnitude constant. When observed on a spectrum analyzer, amplitude and phase noise appears as sideband noise on both sides of the carrier. Often, phase noise specifications refer to single-sideband noise. Most phase noise measurement schemes fold both sidebands together. Increased phase noise decreases the magnitude of SNR, degrading the overall converter performance.

**Phase Nonlinearity:** Phase nonlinearity is the deviation of the phase response from a linear-phase response as a function of frequency.

**Pipeline Converter:** A pipeline A/D converter consists of a number of consecutive segments. Each segment can execute its operation concurrently with other segments (see [Figure 21](#)). The segments are similar in their function and only resolve one or two bits. Each segment has a sample-and-hold, a low-resolution flash A/D converter, and a summing stage, including an inter-stage amplifier for providing gain. Stage 1 takes a sample of the input voltage and makes the first coarse conversion. The result is then the MSB and its digital value is fed to the first latch (Latch 1). When a segment completes an operation, it passes the analog difference to the next segment. As the residue of the first stage gets resolved in the subsequent  $n$ -stages, the MSB value ripples through the  $n$  number of latches in order to coincide with the end of the conversion of the last stage.

### Pipeline Converter, continued:

As seen in [Figure 21](#), the number of segments is often similar to the number of bits of resolution. The outputs of each stage are combined in the output latch. Then, all data bits are latched in the output and are available on the parallel data bus. This process results in a data latency (see [Figure 1](#)) of several clock cycles (refer to the respective product data sheet).



**Figure 21. Pipeline A/D Converter Topology**

**Pipeline Delay (Latency):** see [Latency, pipeline](#).

**Power Dissipation:** The A/D converter consumes this amount of power as a function of sampling frequency and quiescent current. This value is an important specification for power-sensitive applications and their respective environments, including battery-powered circuits, extreme temperature conditions, and/or space limitations.

**Power Down, hardware:** The voltage that is applied to the A/D converter power pin is removed or made to be equal to 0V. With the power down, software engaged, the power remains applied to the power pin of the device.

**Power Down, software:** In order to invoke a software power down, some A/D converters have a register option that powers down the converter to a quiescent current that is lower than the current flowing during normal operation.

**Power Supply Rejection Ratio (PSRR):** The ratio of a change in the power-supply voltage to resulting bit change. This specification is expressed in dB or  $\mu\text{V/V}$ .

- **DC Power-Supply Rejection Ratio (DC PSRR or PSRR)—**

DC PSRR is the ratio of output code change (converted to input voltage) to the dc change in power-supply voltage.

- **AC Power-Supply Rejection Ratio (AC PSRR)—**

AC PSRR is the ratio of the output spectral power with respect to the injected ac-power on the positive supply pin at that frequency, displayed on an FFT plot. The ac-input amplitude on the power supply should be limited to less than  $100\text{mV}_{\text{PP}}$ . This specification is expressed in dB.

**Programmable Gain Amplifier (PGA):** A programmable gain amplifier is an analog amplifier with digitally-programmed gain.

**Quantization:** Quantization occurs when a continuous range of analog input values are divided into non-overlapping sub-ranges. Each sub-range becomes a unique, discrete value at the output of the A/D converter. This specification sets the theoretical limit of the converter SNR. (See [Signal-to-Noise Ratio](#).)

**Quantization Noise:** The noise that an A/D converter generates as a consequence of dividing the input signal into discrete *buckets*. The ideal width of these *buckets* is equal to the LSB size of the converter. The uncertainty of any A/D converter bit is  $\pm 1/2$  LSB. This characterization is true for a perfect converter with no Differential Non-Linearity (DNL) errors. If it is assumed the response of this error is a triangular across an analog input signal, the rms value of the triangular signal is equal to the magnitude of signal divided by the  $\sqrt{3}$ .

$$\text{Quantization Noise (rms)} = \frac{\pm (\text{LSB})}{\sqrt{3}} = \frac{q}{\sqrt{12}}$$

With:

- q = ideal code width

**Ratiometric Operation:** This term describes an environment where the converter uses the same reference voltage as is used to drive the signal source, such as a sensor. Under these conditions, the output code is a function of the ratio of reference voltage to the signal source and is independent of the value of the reference voltage.

**Record of Data:** A record of data is a collection of samples that are acquired in a sequential fashion from an A/D converter.

**Resolution:** When describing the general performance of a converter, resolution is the number of possible output bits that an A/D converter can produce in one conversion. Resolution also is the smallest analog increment corresponding to a 1LSB converter change. This critical specification determines the smallest analog input signal that can be resolved.

**Rise Time:** Rise time is the time required for a signal to rise from 10% of the transition range to 90% of that range.

**Root-mean-square (rms):** RMS is a mathematical term for the standard deviation from a record of data. The calculation of rms is equivalent to the square root of the arithmetic mean of the squared values (the difference between the data and the mean).

**Root-sum-square (rss):** For a given set of data, rss is the square-root-of-the-sum-of-the-squares.

**Sampling:** Sampling assigns discrete time values to a continuous time signal.

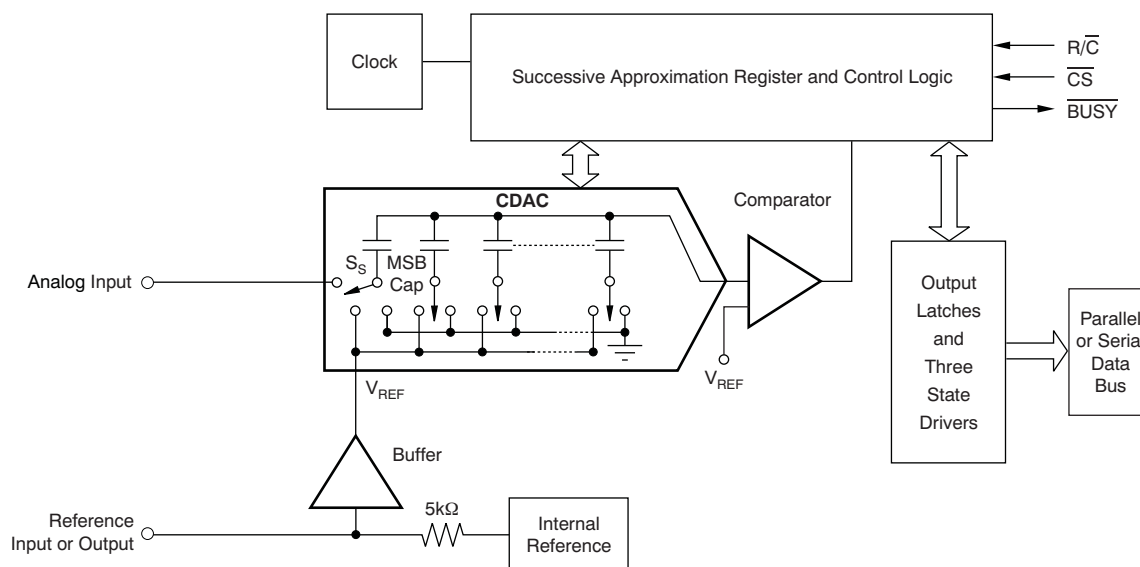
**Sample-and-Hold (or S&H):** A sample-and-hold circuit has an analog-switched input with a function that opens (samples) for a short duration to capture (hold) the analog input voltage.

**Sampling Time:** Sampling time is the time required to sample an analog input signal to a specified level of accuracy. Also see [Acquisition Time](#).

**Sample Rate:** The Sample Rate is the speed that a converter can continuously convert several conversions. This critical specification determines the largest allowable bandwidth of the analog input signal. Typically specified as samples per second (sps) or hertz (Hz). (Also see [Conversion Maximum Rate](#).)

**SAR Converter:** Successive-approximation register (SAR) converters are frequently the architecture of choice for medium-resolution applications with medium sampling rates. SAR A/D converters range in resolution from 8 bits to 18 bits with speeds typically less than 10MSPS. They provide low power consumption and have a small form factor. [Figure 22](#) illustrates a typical SAR converter architecture.

### SAR Converter, continued:



**Figure 22. Successive Approximation Register A/D Converter Block Diagram**

In more recent designs, the topology of SAR A/D converters use a capacitive redistribution design approach instead its predecessor architecture, the R-2R ladder topology. The capacitive-redistribution, SAR converter uses a capacitive array at the analog input (see [Figure 22](#)). The capacitive array and the remainder of the device can be manufactured in a CMOS process, making it easy to integrate the SAR converter with microcontrollers or microprocessors. With the topology shown in [Figure 22](#), the analog input voltage is initially sampled by connecting the input signal to the bottom side of sampling capacitors. This configuration is achieved with the sampling switch ( $S_s$ ). The other ends of these sampling capacitors are connected to the reference voltage. Once the capacitors are fully charged from the analog input voltage, the internal capacitive array of the converter is disconnected from the input signal as well the voltage reference.

Now that the input signal has been sampled, the bottom side of the MSB capacitor is connected to the reference voltage while the other capacitors are tied to the system ground. With this action, the charge from the MSB capacitor is distributed among the other capacitors. The comparator input moves up or down in voltage according to the way the charge is distributed. If the voltage across the capacitive array is greater than the comparator reference, an MSB equal to zero is generated and the MSB capacitor is left tied to  $V_{REF}$ . If this voltage is less than the comparator reference, an MSB bit equal to '1' is generated, and the MSB capacitor is connected to ground.

With the determination of the value of the MSB, the converter then examines the MSB–1 value. This process is done by connect the MSB–1 capacitor to the voltage reference while the other capacitors are tied to ground. Once again, a comparison of this voltage to the internal voltage reference is done with the comparator. In this analysis, if this voltage is greater than the comparator reference, an MSB–1 equal to zero is generated and the MSB–1 capacitor is left tied to  $V_{REF}$ . If this voltage is less than the comparator reference, an MSB–1 bit equal to one is generated and the MSB–1 capacitor is connected to ground. This process is repeated until the capacitive array is fully utilized.

The SAR architecture is ideal for applications where a multiplexer may be used before to the converter, applications where the converter may only need to make a measurement once every few seconds, or applications that require a *fast* measurement. The conversion time remains the same in all cases and has little sample-to-conversion latency compared to a pipeline or delta-sigma converter. SAR converters are ideal for real-time applications such as industrial control, motor control, power management, portable/battery-power instruments, PDAs, test equipment, and data/signal acquisition.

**Second Harmonic (HD2):** The second harmonic is two times the frequency of the fundamental.

**Settling Time** (as it relates to  $\Delta\Sigma$  A/D converters): The settling time of the digital filter in a delta-sigma A/D converter reflects the order of the digital filter internal to the converter. This *time* is given in cycles and equal to the number of conversions required for the signal to propagate through the filter. Settling time can be an issue to consider after power-up, when switching channels with the input multiplexer, after an input step response, or re-starting the converter after a long wait time.

**Signal-to-Noise Ratio (SNR):** The signal-to-noise ratio is a calculated rms value that represents the ratio of ac signal power to noise power below one-half of the sampling frequency. The noise power excludes harmonic signals and dc.

The ideal SNR for SAR and pipeline converters with a full-scale sine wave input to an A/D converter is  $6.02n + 1.76\text{dB}$ ;  $n$  is equal to the number of converter bits. SNR can be specified with respect to full-scale input range (dBFS or dB) or with respect to the actual input signal amplitude (dBc). The three different formulas for SNR are:

$$\text{SNR (dB)} = 10\log_{10} \frac{P_S}{P_N}, \text{ where } P_S \text{ is the signal power and } P_N \text{ is the noise power.}$$

$$\text{SNR (dB)} = 10\log_{10} \frac{\text{rms signal}}{\text{rms noise}}$$

$$\text{SNR (dB)}_{\text{ideal}} = 10\log_{10} \left[ \frac{(2^{(n-1)} \cdot \frac{q}{\sqrt{2}})}{\frac{q}{\sqrt{12}}} \right] = 6.02n + 1.76 \text{ (dB)}$$

Where:

- $q$  = the LSB size
- $n$  = number of bits

The ideal SNR for a delta-sigma converter first-order modulator is  $6.02n + 1.76\text{dB} + 10\log_{10}(f_s / (2BW))$ , where  $f_s$  is the converter sampling frequency and  $BW$  is the maximum frequency of interest.

Other dynamic or ac specifications include the [Signal-to-Noise Ratio plus Distortion \(SINAD or SNR+D\)](#), [Effective Number Of Bits \(ENOB\)](#), [Total Harmonic Distortion \(THD\)](#), [Spurious Free Dynamic Range \(SFDR\)](#), [Intermodulation Distortion \(IMD\)](#), and [Full-power Bandwidth \(FPBW\)](#). (Also see [Quantization Noise](#).)

**Signal-to-(Noise Ratio plus Distortion) (SINAD or SNR+D, also called Total Harmonic Distortion plus Noise):** SINAD is the calculated combination of SNR and total harmonic distortion (THD). SINAD is the ratio of the rms amplitude of the fundamental input signal to the rms sum of all other spectral components below one-half of the sampling frequency (excluding dc). The theoretical minimum for SINAD is equal to the ideal SNR or  $6.02n + 1.76\text{dB}$  with SAR and pipeline converters.

$$\text{SINAD} = -20\log_{10} \sqrt{(10^{-\text{SNR}/10} + 10^{+\text{THD}/10})} \quad \text{or}$$

$$\text{SINAD} = 10\log_{10} \left[ \frac{P_S}{P_N + P_D} \right]$$

Where:

- $P_S$  is the fundametal signal power;
- $P_N$  is the power of all the noise spectral components; and
- $P_D$  is the power of all the distortion spectral components

SINAD is either given in units of dBc (decibels to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (decibels to full-scale) when the power of the fundamental is extrapolated

to the converter full-scale range. SINAD is a critical specification for digital oscilloscope/waveform recorders, as well as geophysical, image processing, radar, sonar, spectrum analysis, video, telecommunication, and wideband digital receiver applications. Other dynamic or ac specifications include the [Signal-to-Noise Ratio \(SNR\)](#), [Effective Number Of Bits \(ENOB\)](#), [Total Harmonic Distortion \(THD\)](#), [Intermodulation Distortion \(IMD\)](#), and [Full-power Bandwidth \(FPBW\)](#).

**Small Signal:** A voltage input signal whose peak-to-peak amplitude spans not more than 10% of the full input range of the A/D converter.

**Spurious Free Dynamic Range (SFDR):** The distance in dB on an FFT plot from the fundamental input signal to the worst or highest spur. SFDR can be specified with respect to full-scale input range (dBFS or dB), or with respect to the actual input signal amplitude (dBc). (See [Figure 23](#).) SFDR is a critical specification for telecommunication and video applications. Other dynamic or ac specifications include the [Signal-to-Noise Ratio \(SNR\)](#), [Signal-to-Noise Ratio plus Distortion \(SINAD or SNR+D\)](#), [Effective Number Of Bits \(ENOB\)](#), [Total Harmonic Distortion \(THD\)](#), [Intermodulation Distortion \(IMD\)](#), and [Full-power Bandwidth \(FPBW\)](#).

**Static Specifications:** Static specifications are the A/D converter specifications pertaining to a dc signal input. These specifications generally include [Offset Error](#), [Gain Error](#), [DNL](#), [INL](#), and [TUE](#).

**Step Response:** The step response is the time required for the output digital results to reflect the rated accuracy of the converter after the input voltage goes from the lowest input voltage to the highest input voltage (or vice-versa).

**SPI (Serial Peripheral Interface):** See [Digital Interface SPI](#).

**Successive Approximation Register Converter (SAR):** See [SAR Converter](#).

**Synchronous Sampling:** Synchronous sampling is where the input signal is phase locked to the sampling of another signal and/or to the A/D converter sampling frequency.

**Temperature, Specified:** The temperature range where electrical specifications apply. If the device is taken beyond the specified temperature range, the typical, maximum, and minimum specifications do not apply.

**Temperature, Storage:** The temperature range limiting storage conditions. If the device is stored at temperatures beyond the stated storage temperatures, damage to the device may occur.

**Temperature, Junction:** The maximum allowed internal junction temperature. If this junction temperature is exceeded, the device may stop operation and/or damage may occur.

**Temperature, Operating:** The temperature range limits where the product continues to operate, but not necessarily to specification.

**Thermal Noise:** Thermal Noise is generated by a resistor. Ideally, this noise is equal to:

$$\text{Thermal Resistor Noise} = \sqrt{4kTRB}$$

Where:

- k = Boltzmann's constant,  $1.38 \times 10^{-23}$ ;
- T = temperature in degrees Kelvin; and
- B = bandwidth

**Thermal Impedance:** Thermal impedance quantifies a component or device capability to dissipate heat. In electronics, this heat is normally generated by the device power. With components, the overall thermal impedance causes a rise in temperature that is linearly dependent on the power dissipated in the device. The coefficient is called  $\theta$ , and has the units of  $^{\circ}\text{C}/\text{W}$ .

**Third Harmonic (HD3):** The third harmonic is three times the frequency of the fundamental.

**Throughput rate:** Throughput rate is the inverse of throughput time.

**Throughput Time:** The time required for the converter to sample, acquire, digitize, and prepare for the next conversion. This time is also the minimum conversion time in a continuous conversion application.

**Timing Jitter:** See [Aperture Jitter](#).

**Timing Phase Noise:** See [Aperture Jitter](#).



**Total Harmonic Distortion (THD):** The rms sum of the powers of the harmonic components (spurs) ratioed to the input signal power. This ratio is specified in rms decibels (dB) or rms dBc. The formula describing THD is:

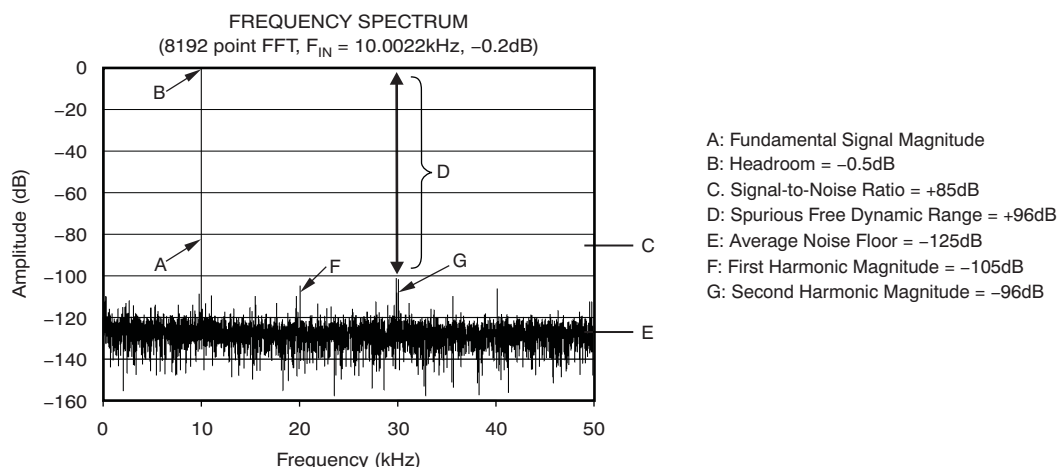
$$\text{THD}_{\text{RMS}} = 20\log_{10} \sqrt{((10^{\text{HD2}/20})^2 + (10^{\text{HD3}/20})^2 + (10^{\text{HD4}/20})^2 + \dots)} \quad \text{or}$$

$$\text{THD}_{\text{RMS}} = \frac{P_S}{P_O}$$

Where:

- $P_S$  = power of the first harmonic (signal power); and
- $P_O$  = power of the first specified harmonics
- HD2 = magnitude of the second harmonic

Significant INL errors of the A/D converter typically appear in the THD results. THD is usually specified with the input signal close to full-scale; see [Figure 23](#).



NOTE: THD is the aggregate of harmonics (F, G, etc.) above the fundamental input signal (A).

**Figure 23. Total Harmonic Distortion FFT Plot**

THD is either given in units of dBc (decibels to carrier) when the absolute power of the fundamental is used as the reference, or dBFS or dB (decibels to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range. THD is a critical specification for geophysical applications. Other dynamic or ac specifications include the [Signal-to-Noise Ratio \(SNR\)](#), [Signal-to-Noise Ratio plus Distortion \(SINAD or SNR+D\)](#), [Effective Number Of Bits \(ENOB\)](#), [Spurious Free Dynamic Range \(SFDR\)](#), [Intermodulation Distortion \(IMD\)](#), and [Full-power Bandwidth \(FPBW\)](#).

**Total Harmonic Distortion plus Noise:** See [Signal to noise ratio plus distortion](#).

**Total Unadjusted Error (TUE):** TUE is a dc specification that determines the overall deviation of digital code as it differs from ideal. This error includes [Offset](#), [Gain](#), and nonlinearity errors in its calculation.

$$\text{TUE} = \text{OFFSET} + \text{GAIN} + \text{INL} + \text{DNL}$$

**Transfer Function (transfer curve):** An A/D converter representation of the average digital output code compared to the analog input value. (See [Figure 10](#))

**Transition Point:** The analog input voltage at which the digital output switches from one code to the next. (See [Figure 10](#))

**Transition Noise:** See [Code Transition Point and Uncertainty](#).

**Two-Tone Intermodulation Distortion:** See [Intermodulation Distortion \(IMD\)](#).



**Undersampling:** In an undersampling system, the sampling rate of the A/D converter is lower than the input frequency, causing aliasing to lower frequencies. With undersampling circuits, the bandwidth of the signal of interest ( $\Delta f_{\text{SIG}}$ ) is centered at a higher frequency than the sampling frequency ( $f_{\text{SAMPLE}}$ ) of the converter:

$$f_{\text{SAMPLE}} > 2 (\Delta f_{\text{SIG}})$$

$\Delta f_{\text{SIG}}$  is limited by an analog bandpass filter that acts like an anti-aliasing filter in this system. The bandwidth of the sample-and-hold (or track-and-hold) function of the input of the A/D converter must be capable of handling these high-frequency signals.

**Uncertainty:** Refer to [Code Transition](#) and [Noise](#).

#### Unipolar Offset:

- **Error–**  
See [Offset Error](#).
- **Drift–**  
See [Offset Error](#).

#### Unipolar Gain:

- **Error–**  
See [Gain Error](#).
- **Drift–**  
See [Gain Error](#).

**Unipolar Straight Binary Code (USB):** With the lowest input voltage, the digital count begins with all zeros and counts up sequentially all ones with a full-scale input. Straight Binary is a digital coding scheme for unipolar voltages only. The representation of 0V is equal to a digital (0000, for a 4-bit system). The analog full-scale  $-1\text{LSB}$  digital representation is equal to (1111). With this code, there is no digital representation for analog full-scale. See [Table 7](#).

**Table 7. Unipolar Straight Binary Code<sup>(1)(2)</sup>**

MNEMONIC	DIGITAL CODE	$V_{\text{TR-}}$	$V_{\text{CODE}}$	$V_{\text{TR+}}$
Zero	0000	—	0.000	0.3125
$+1V_{\text{LSB}}$	0001	0.3125	0.625	0.9375
	0010	0.9375	1.250	1.5625
	0011	1.5625	1.875	2.1875
$1/4$ FSR	0100	2.1875	2.500	2.8125
	0101	2.8125	3.125	3.4375
	0110	3.4375	3.750	4.0625
	0111	4.0625	4.375	4.6875
$1/2$ FSR	1000	4.6875	5.000	5.3125
	1001	5.3125	5.625	5.9375
	1010	5.9375	6.250	6.5625
	1011	6.5625	6.875	7.1875
$3/4$ FSR	1100	7.1875	7.500	7.8125
	1101	7.8125	8.125	8.4375
	1110	8.4375	8.750	9.0625
+FS	1111	9.0625	9.375	—

<sup>(1)</sup> Also known as *straight binary*; FS = 10V.

<sup>(2)</sup>  $V_{\text{TR-}}$  = lower code transition voltage;  $V_{\text{TR+}}$  = upper code transition voltage;  $V_{\text{CODE}} = (\text{digital code})_{10} \times V_{\text{LSB}}$ ;  $V_{\text{TR+}} = V_{\text{CODE}} + (1/2)V_{\text{LSB}}$ ;  $V_{\text{TR-}} = V_{\text{CODE}} - (1/2)V_{\text{LSB}}$ .

**Voltage Reference (also known as Analog Voltage Reference):** This reference voltage sets the analog input range. For the actual analog input range for a given device, refer to the product data sheet. The source of this voltage can be internal or external to the A/D converter.

- **Reference Error—**

The reference error is the variation of the actual reference voltage ( $V_{REFP} - V_{REFM}$ ) or  $V_{REF}$  from its ideal value. The reference error is typically given as a percentage or absolute voltage.

**Zero-Scale Error (or zero-code error):** See [Offset Error \(Unipolar\)](#).

## References

The following documents are available for download through the Texas Instruments web site ([www.ti.com](http://www.ti.com)), except where noted.

- Albanus, J. (2000.). Coding schemes used with data converters. Application report [SBAA042](#).
- Anonymous. (1995.) Understanding data converters. Application report [SLAA013](#).
- Baker, B. (2005.). [A Baker's Dozen: Real analog solutions for digital designers](#). Burlington, MA: Elsevier/Newnes.
- Institute of Electrical and Electronics Engineers, Inc. (2001.). IEEE STD-1241-2000: IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters. Available at [IEEE.org](http://IEEE.org).
- Oljaca, M. and Hendrick, T. (2004.). Data converters for industrial power measurement. Application report [SBAA117](#).

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