Digital FIR Filter Design Using the MSP430F16x

Murugavel Raju   *MSP430*

ABSTRACT

This application report describes an FIR filter implementation using the MSP430F16x and the MSP430F161x family devices. The complete filter algorithm is executed by the 3-channel DMA peripheral and the hardware multiplier peripheral. These modules are used in conjunction with the allocated coefficient table in the program memory and the circular data buffer space dedicated in the RAM of the device. The hardware multiplier performs the signed multiply-and-accumulate (MACS) operations in the algorithm. The integrated analog-to-digital converter, ADC12, is used for data acquisition. The software for the filter is written in such a way that all the filter parameters including the coefficients are loaded into a look-up table. This allows the same filter program to be used for any type of FIR filter implementation such as high-pass, low-pass, band-pass and band-reject filters. The integrated digital-to-analog converter, DAC12, can be used for converting the filter output back into the analog domain if required.

1   Theory of Operation

Digital finite impulse response (FIR) filters form the basis for numerous digital signal processing applications. The basic operation needed to implement a FIR filter is the signed multiply-and-accumulate (MACS), which is traditionally performed using a hardware multiplier peripheral in any DSP device. Some of the MSP430 devices have an integrated hardware multiplier that can perform this MACS operation allowing these devices to run the FIR filter algorithm more efficiently than devices without a built-in hardware multiplier.

Equation 1 shows a mathematical expression for the FIR filter,

$$y(k) = \sum_{i=0}^{N} \alpha i \times x(k - i)$$

(1)

where k is the time step, y(k) is the filter output at time k, x(k–i) is the sampled input at time k–i, ai is the filter coefficient i, and N is the order of the filter (= number of taps −1).

In addition to the MACS operation the processor handles the task of moving the digital samples and filter coefficients from memory to the MAC hardware, retrieving the results and storing them into memory. In a real-time digital filter algorithm, the computation and memory-move operations have to be completed within one sample period. The number of computations to be performed within one sample period depends on the number of taps of the filter, i.e, the order of the filter. The order of the filter is determined by the required filter performance characteristics. When higher order filters are combined with faster sampling rates, the demand on the processor becomes very high. This limits typical MCU's to handle a real-time FIR filter algorithm only at low sample rates and with a reduced number of filter taps.

The MSP430F169 with its rich peripheral set handles the FIR filter algorithm in a different manner compared to conventional MCUs. This device has a three channel DMA peripheral that handles the required data, coefficient and result movement between the memory and the MAC, dramatically improving the computation efficiency of the real-time FIR filter algorithm running on-chip.

The DMA peripheral completes a memory transfer operation in two CPU clock cycles. Additionally it has software-selectable trigger sources that make it ideally suitable for the FIR filter implementation. The FIR filter runs on the DMA-MACS-Memory combination autonomously without the intervention of the CPU. The CPU is primarily only being used for the initialization of peripherals.

The coefficients of the FIR filter are symmetrical in nature. Due to this the coefficient table size can be reduced to half the number of taps of the filter. In a DSP device the input sample data is stored in a circular buffer to implement the movement of the samples through the FIR computation blocks without having to literally move the data in memory. When a new sample is added to the buffer, it automatically replaces the oldest one. A similar circular buffer arrangement is made in the linear memory space of the MSP430 by a folded address structure approach using DMA channels 1 and 2. Figure 1 represents the block diagram of the FIR filter implementation in the MSP430F169.
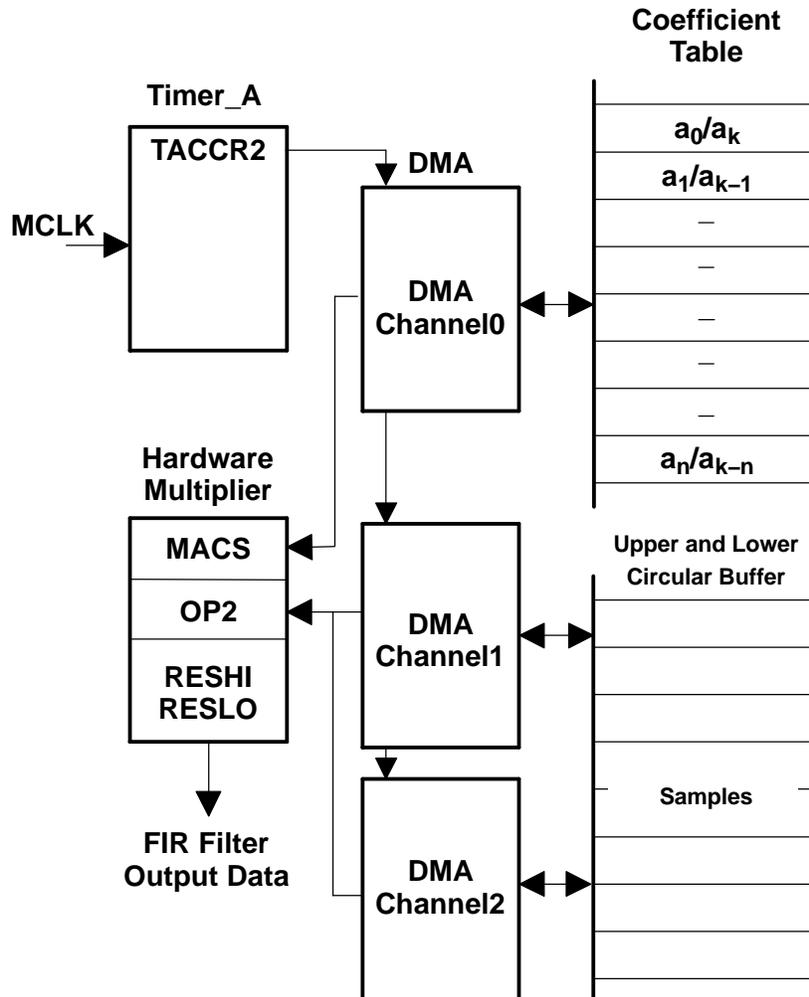
Figure 1. FIR Implementation Using the MSP430F169

2 FIR Filter Software Algorithm

The FIR filter software for the MSP430F169 is written in assembly language to achieve maximum performance. The software is written to accept the coefficients stored in the form of a look-up table pointed to by the label *FILTER* in program memory. The first value in the look-up table is the value for Timer_A for the required sampling frequency. The next value is the number of filter taps N and the remaining values are filter coefficients.

Table 1 shows the performance that can be achieved using the MSP430F169 with an 8 MHz CPU clock frequency with respect to filter taps and the maximum sampling rate possible with 100% CPU loading.

Table 1. MSP430F169 FIR Filter Benchmarks

Number of Taps, N	Number of CPU Clocks	Maximum Sampling Rate (kHz) (100% CPU loading)
32	310	25
50	410	19
100	730	11

Practical signal processing needs are typically much lower than the maximum possible numbers shown in the table. In such cases more free CPU resources will be available for the user application while running the FIR filter

6   References

1. *Understanding Digital Signal Processing* by Richard G. Lyons
2. *The Scientist and Engineer's Guide to Digital Signal Processing* by Steven W. Smith
3. *MSP430x1xx Family User's Guide* (SLAU049)
4. MSP430x16x Data sheet (SLAS368)

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