MSP430 Advanced Technical Conference 2006

Introduction to MSP430 ADCs

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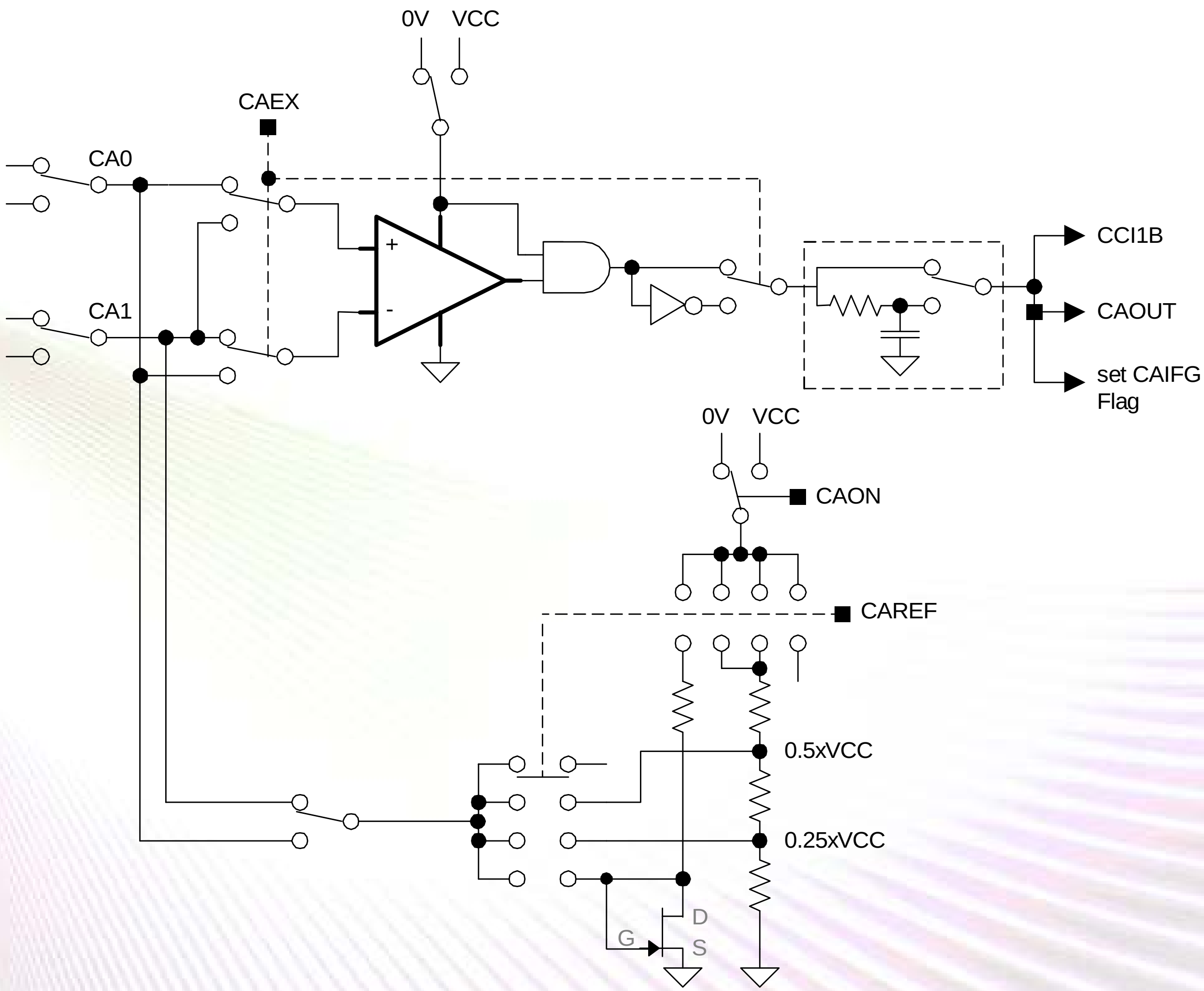
Agenda

- Analog measurements with the MSP430
  - **Comparator, ADC10, ADC12, SD16, SD16_A**
- Hands-on lab with ADC12
- Summary

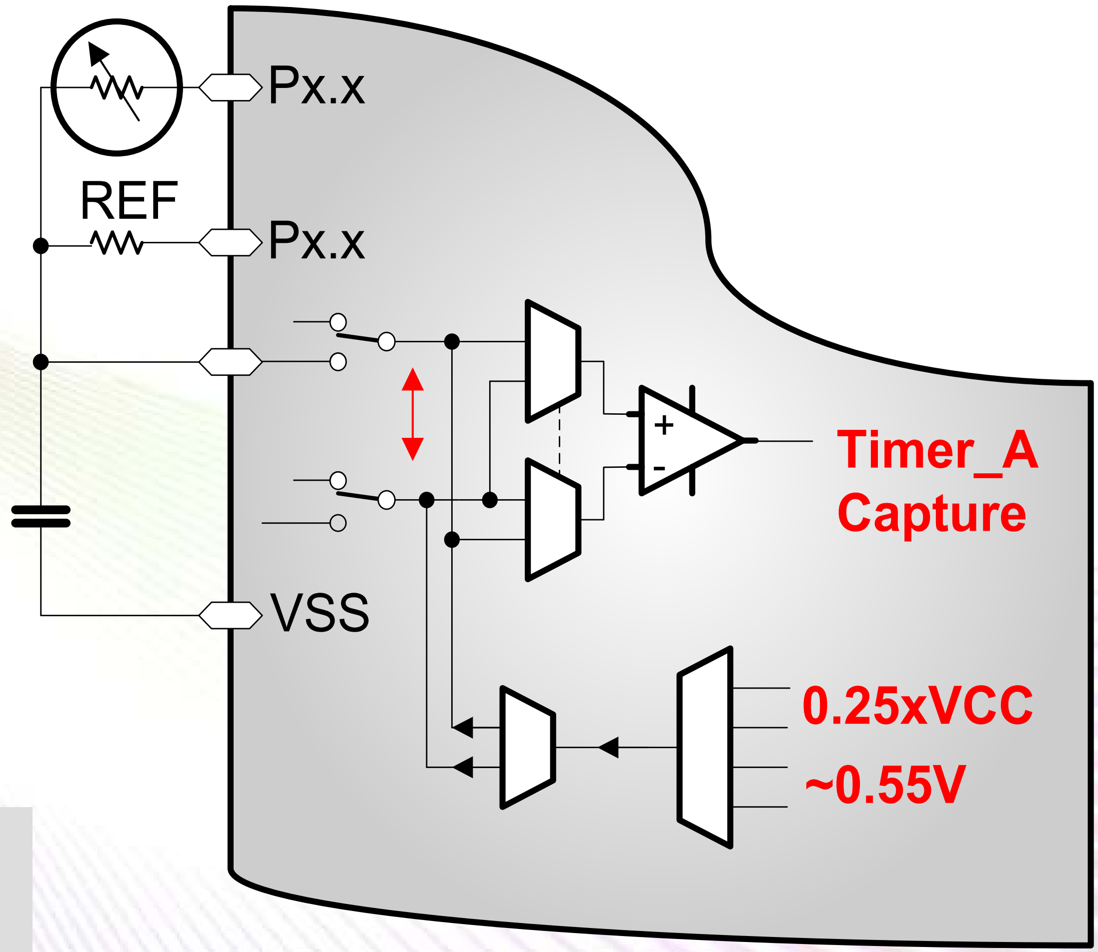
Comparator_A

- **References usable internally and externally**
- **Low-pass filter selectable by software**
- **Input terminal multiplexer**
- **One interrupt vector with enable**



Comparator-Based Slope ADC

- **10-bit+ accuracy**
- **Resistive sensors**
- **Low battery detect**
- **Very low cost**
- **App note SLAA038**



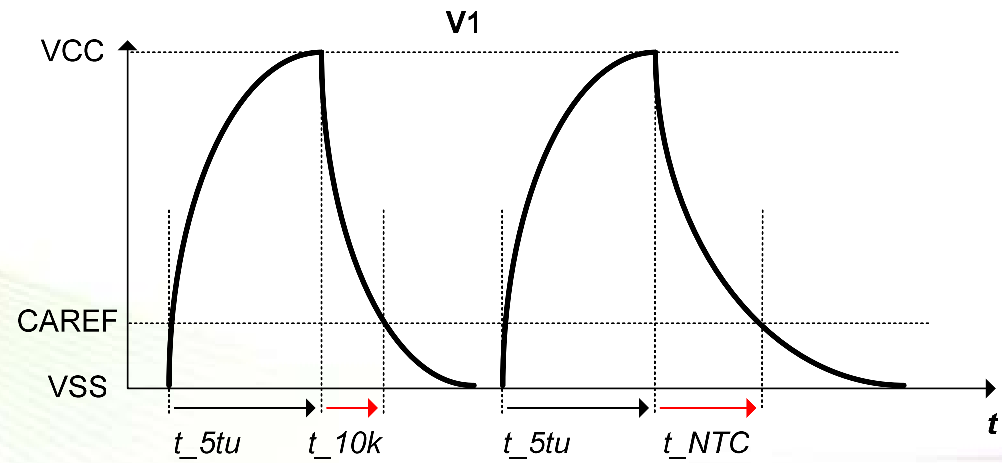
$$t\_x = R\_x \times C \times \ln \frac{VCAREF}{Vcc}$$

. . .

$$R\_NTC = 10k \times \frac{t\_NTC}{t\_10k}$$

Example: Thermistor

- R_{REF} = 10K, R_M = NTC
- $V_{CAREF} = V_{CC} * e^{(-t/RC)}$
- Relationship simplifies to single multiply & divide operations



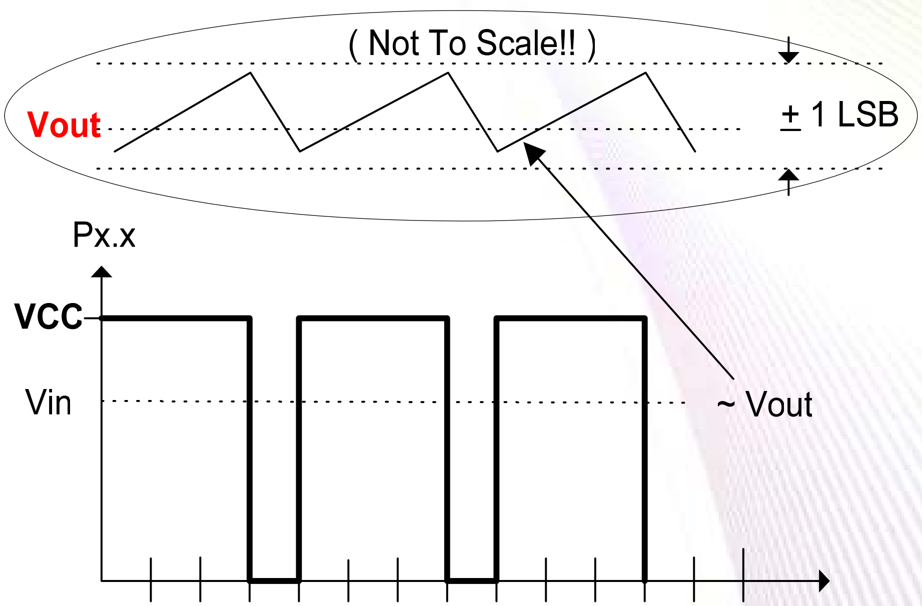
$$\frac{R\_NTC}{10k} = \frac{\dfrac{t\_NTC}{C \times \ln \dfrac{V_{CAREF}}{Vcc}}}{\dfrac{t\_10k}{C \times \ln \dfrac{V_{CAREF}}{Vcc}}} \rightarrow \boxed{R\_NTC = 10k \times \frac{t\_NTC}{t\_10k}}$$

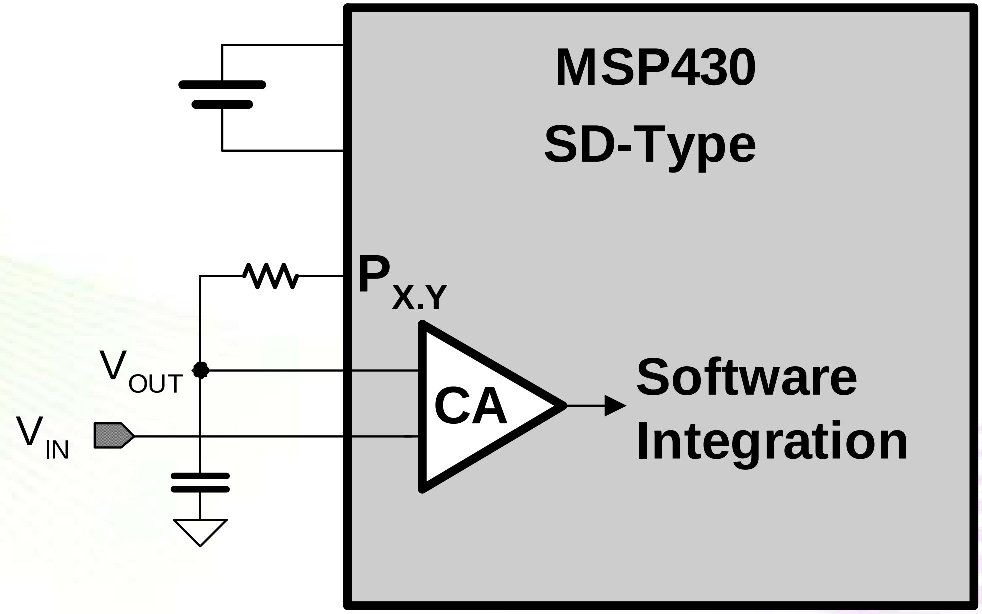
Slope Resistance Considerations

- Measurement as accurate as R_{REF}
- V_{CC} independent
- Resolution based on number of max counts possible
- Precharge of C_M impacts accuracy
- Slope measurement time duration a function of RC

Integrating A/D Voltage Measurement

- V_{IN} range is near full scale
- $P_{X.Y}$ toggling creates a 1-bit DAC at V_{OUT}
- Match V_{OUT} to V_{IN}
- SLAA104





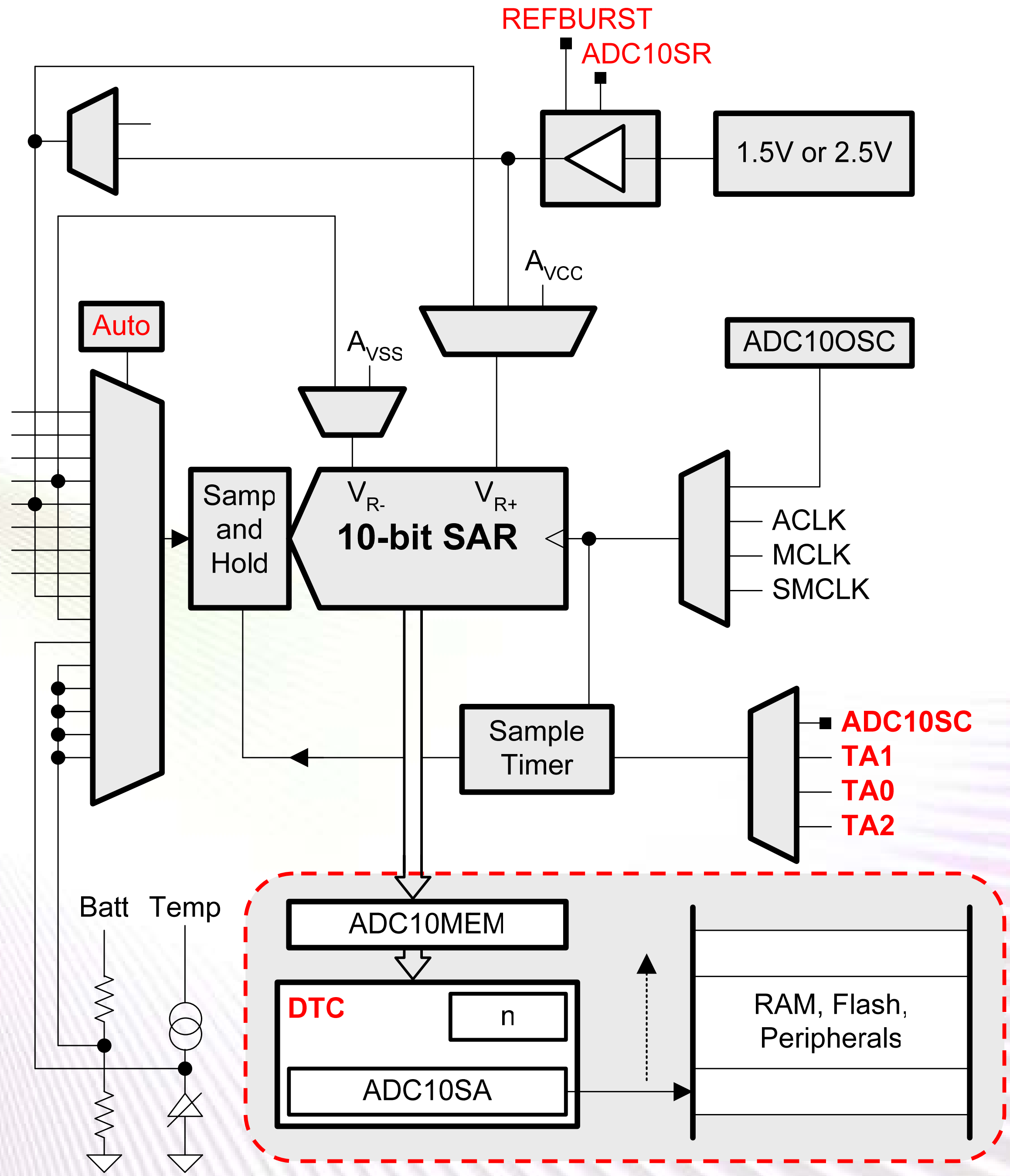
Used for voltage sensors, 10-bit+ resolution as accurate as Vcc

Integrating A/D Considerations

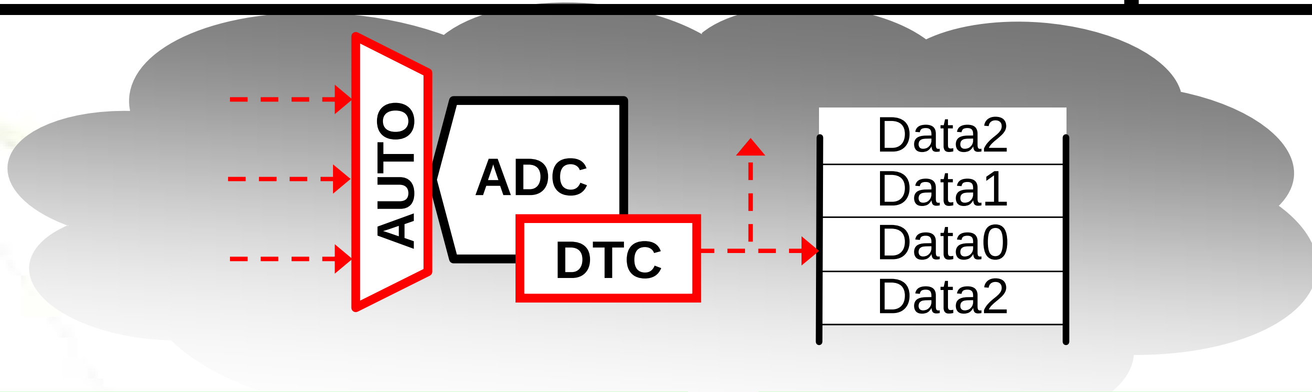
- Resolution determined by times through S/W loop
- Inherently excellent noise immunity
- V_{CC} must be known
- DAC pulse symmetry required
- Select RC values for < +/- 1LSB V_{OUT} ripple
- Reference: SLAA104

ADC10

- 200ksps+
- Autoscan
- Single
  Sequence
  Repeat-single
  Repeat-sequence
- Int/ext reference
- TA SOC triggers
- Data transfer controller
- 30us ref settling, No decoupling required



Why Is Autoscan + DTC Important?




```
// Software
Res[pRes++] = ADC10MEM;
ADC10CTL0 &= ~ENC;
if (pRes < NR_CONV)
 {
 CurrINCH++;
 if (CurrINCH == 3)
   CurrINCH = 0;
 ADC10CTL1 &= ~INCH_3;
 ADC10CTL1 |= CurrINCH;
 ADC10CTL0 |= ENC+ADC10SC;
 }
```

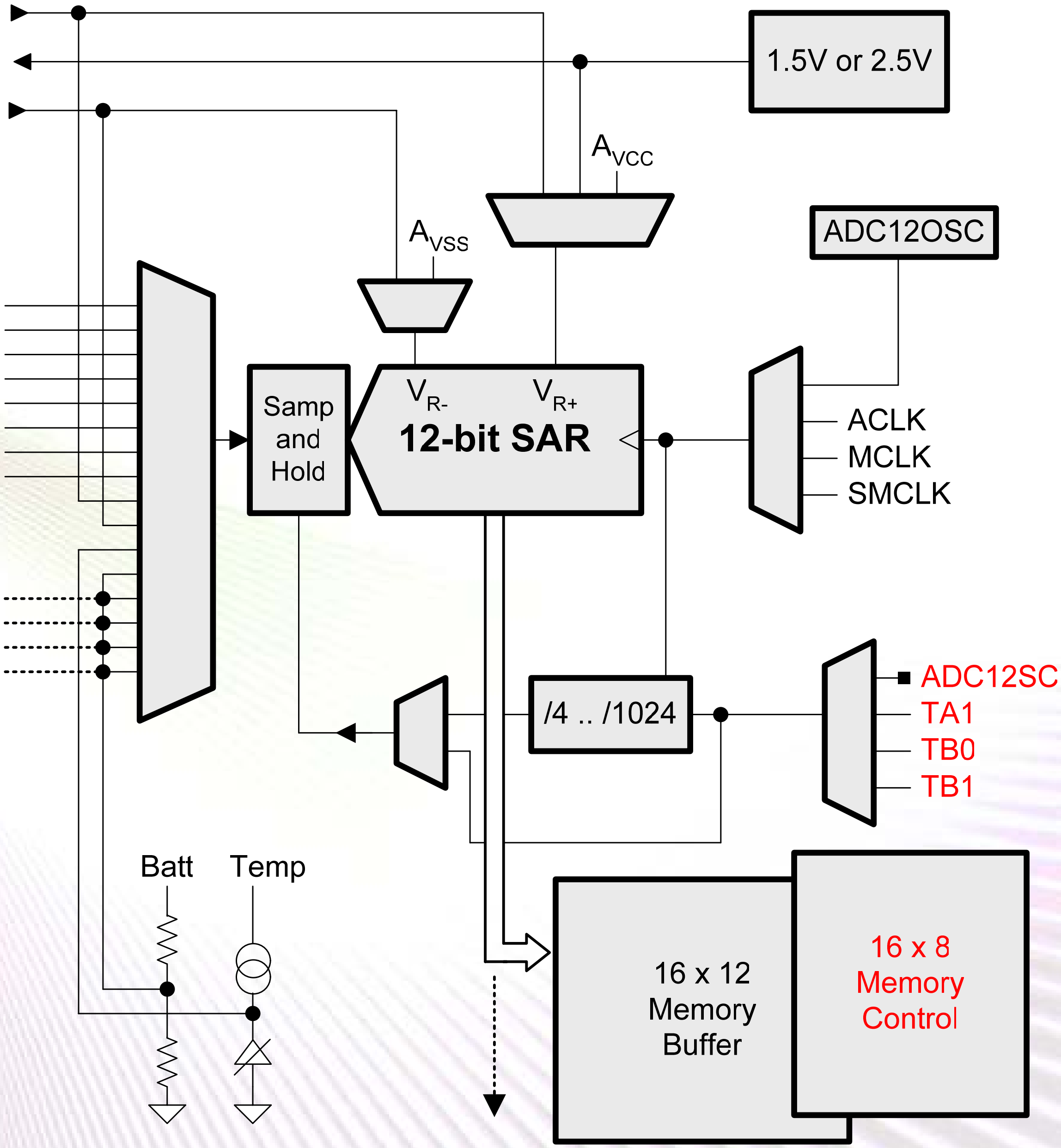
```
// Autoscan + DTC
 _BIS_SR(CPUOFF);
```

70 cycles/Sample

Fully Automatic

ADC12

- 200ksps+
- Single
  Sequence
  Repeat-single
  Repeat-sequence
- Int/ext reference
- TA/TB SOC triggers
- Configuration memory/buffer
- DMA enabled

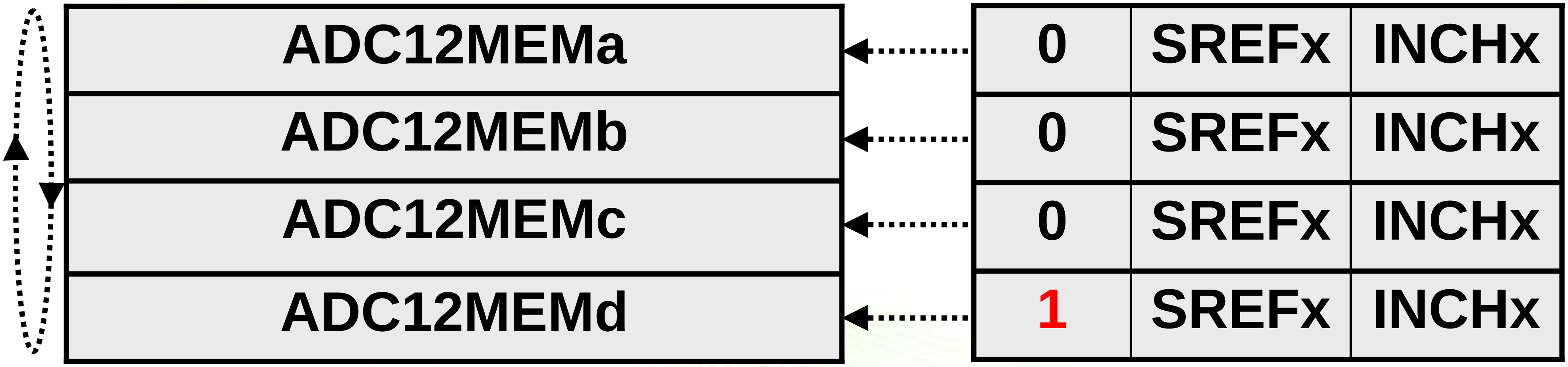


ADC12 Conversion Memory

ADC12MEMx		7	6-4	3-0
ADC12MEM0	←	EOS	SREFx	INCHx
ADC12MEM1	←	EOS	SREFx	INCHx
ADC12MEM2	←	EOS	SREFx	INCHx
⋮				
ADC12MEM15	←	EOS	SREFx	INCHx

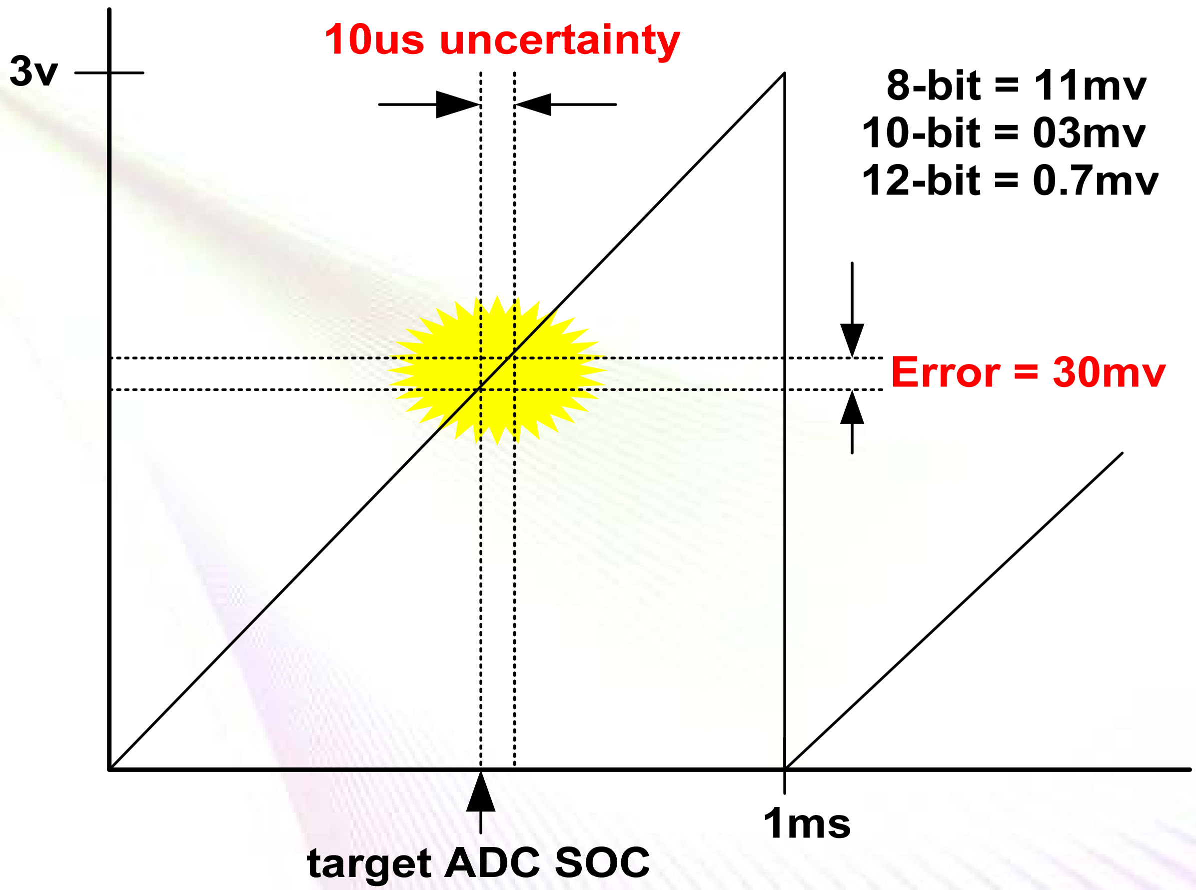
- 16 memory buffer
- Each interrupt capable
- Each DMA enabled

Conversion Sequences



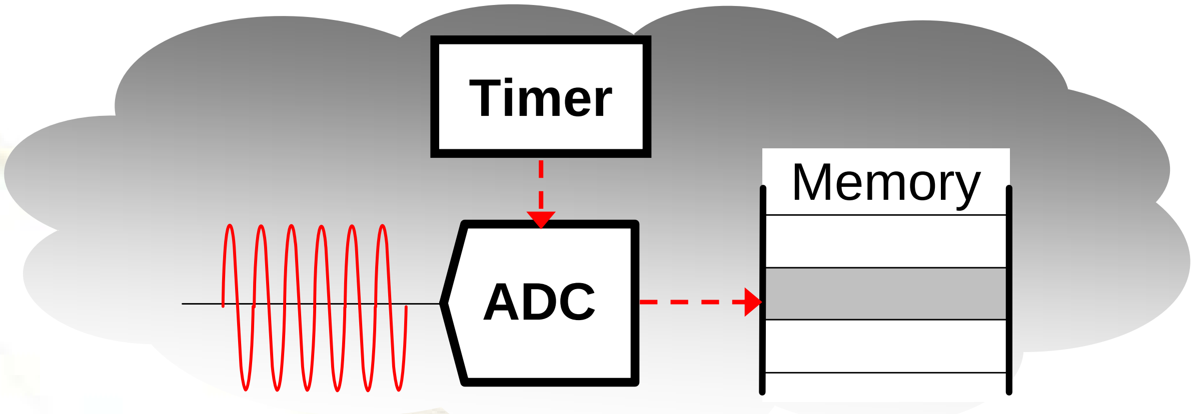
- Single or repeat
- Flexible channel selection
- Complete conversion timing control

Timer SOC Triggers - Accuracy



Automatic SOC trigger eliminates phase error

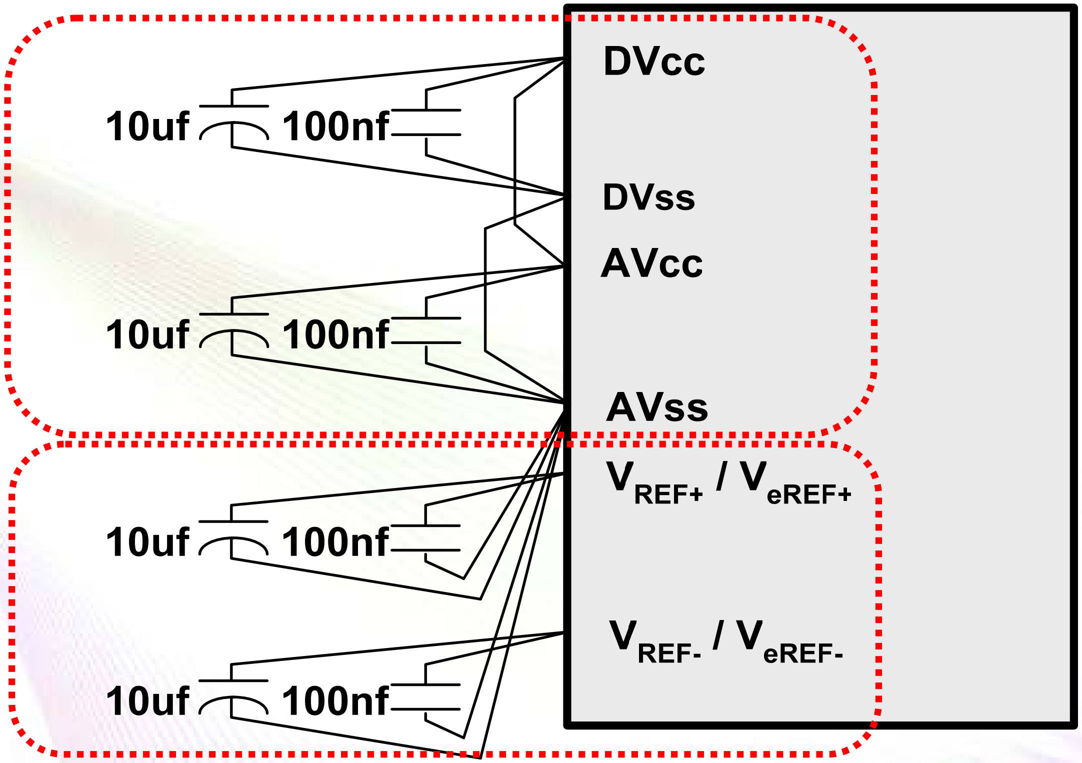
Timer SOC Triggers – Low-Power




```
// Interrupt                                          CPU cycles
; MSP430 ISR to start conversion                          6
BIS   #ADC12SC,&ADC12CTL0 ; Start conversion              5
RETI                      ; Return                        5
                          ;                              16
```

ADC12 Reference Decoupling

- Power Supply
- Any used VRef



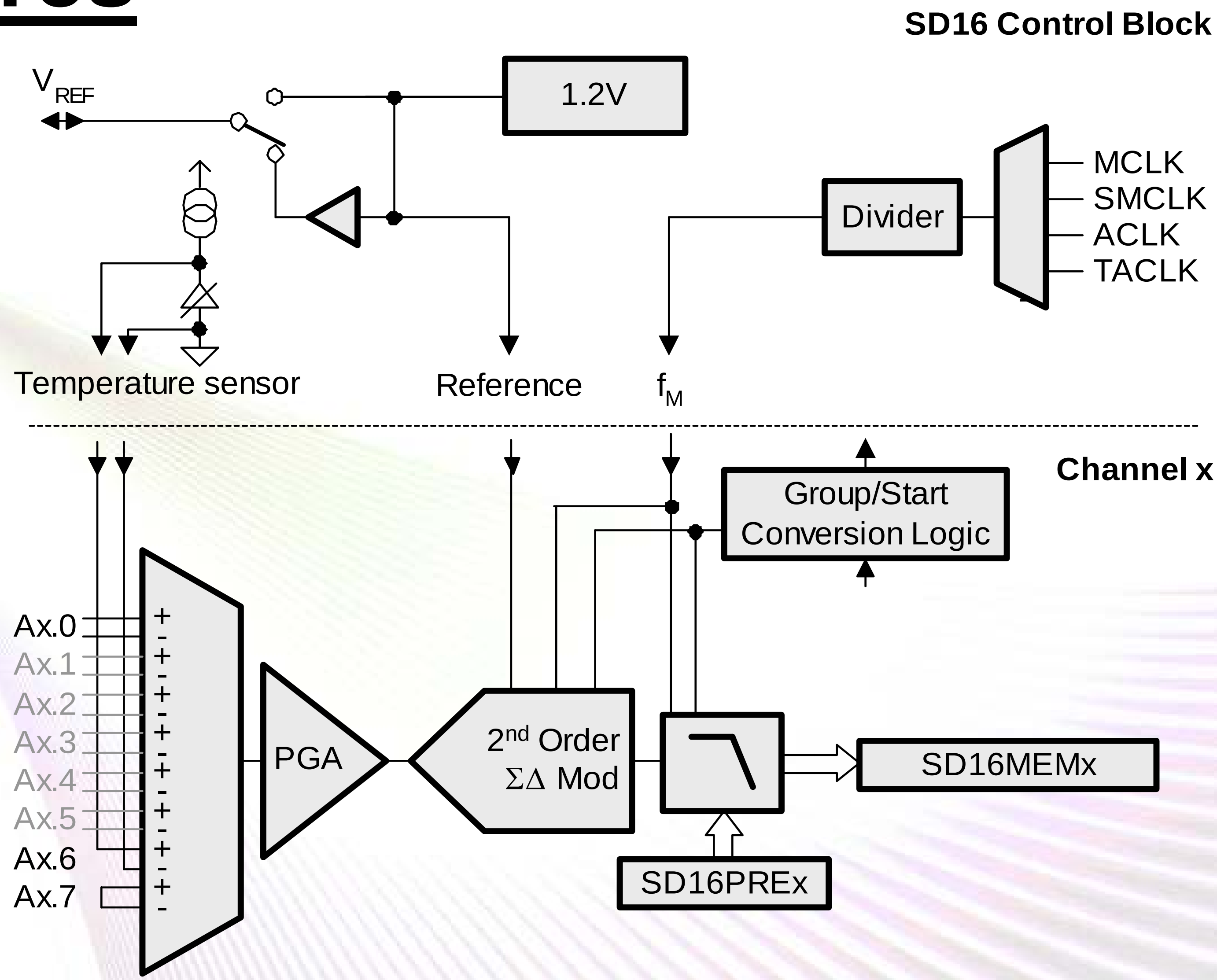
Any used reference must be decoupled with > 5uf

MSP430 SD16 Sigma-Delta Overview

- 16-bit sigma-delta architecture
- Independent converters
- 4096 samples per second
- Differential input
- Independent PGA
- Internal 1.2V reference
- Internal temperature sensor
- Converters can be grouped
- 2.7 – 3.6V

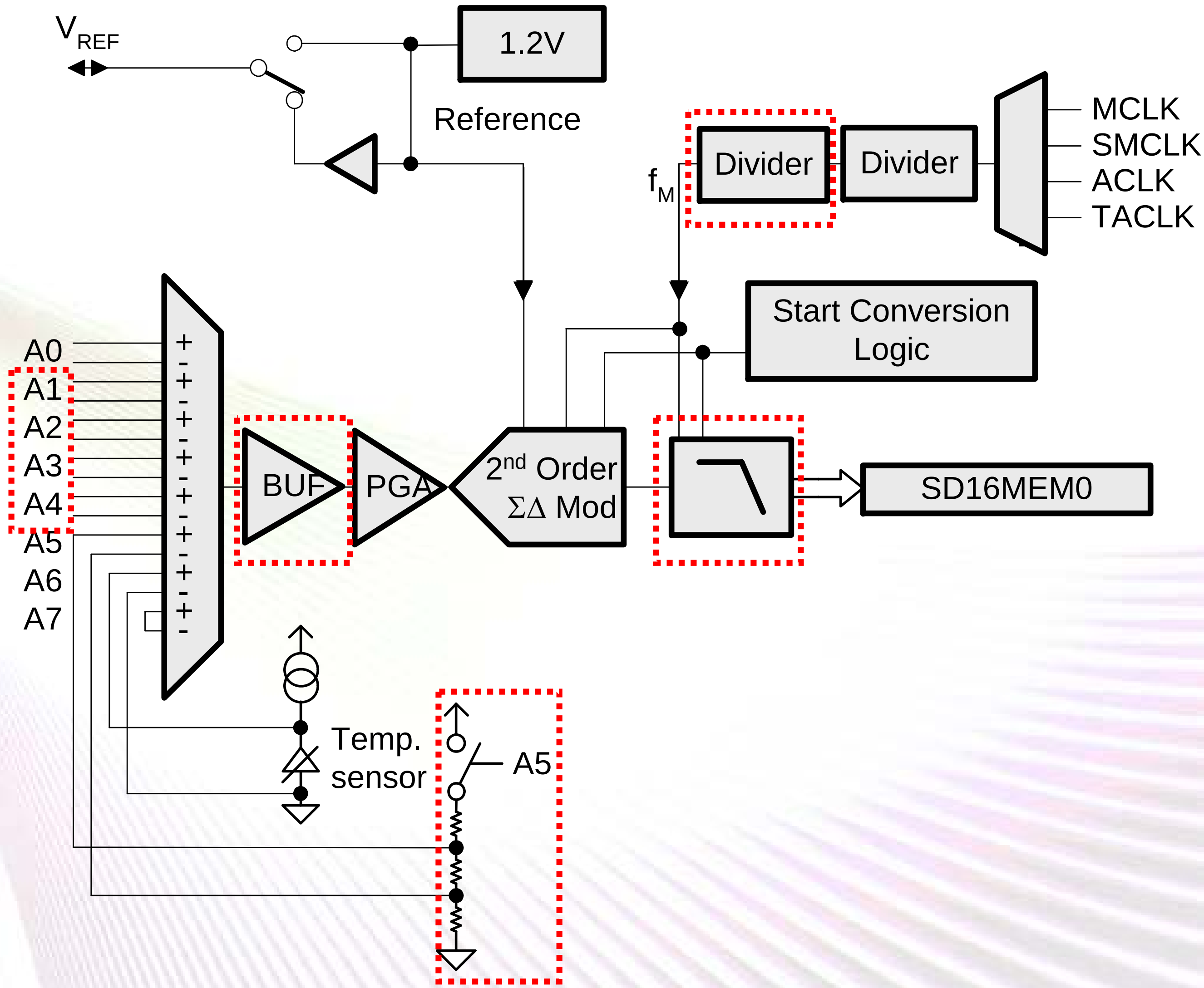
SD16 Features

- 'F42x & 'FE42x
- Multiple channels
- Single external input per channel
- Up to 256 OSR
- 1MHz f_M



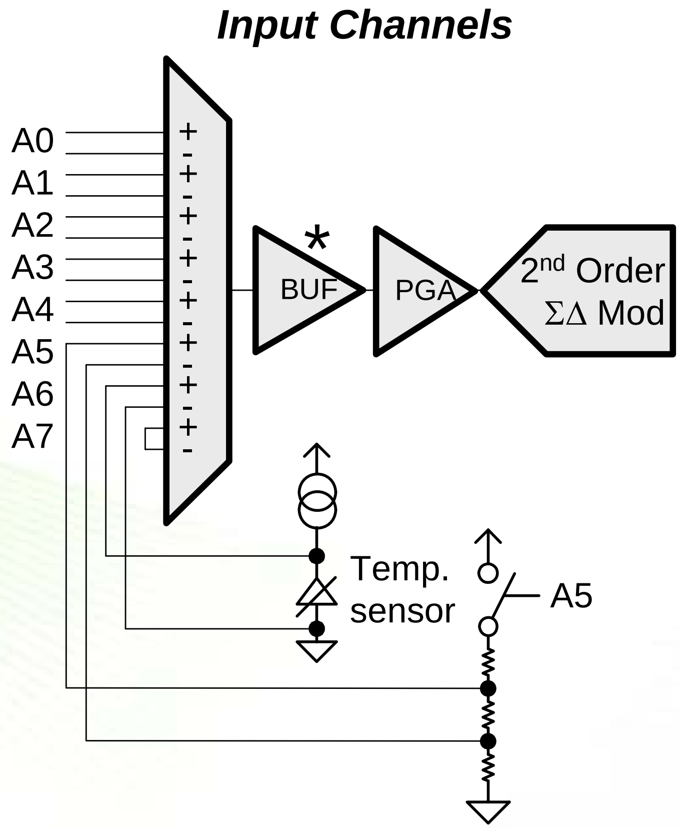
SD16_A Overview

- ‘F42x0 & ‘F20x3
- Single channel
- Multiple input pairs
- Input buffer
- AV_{CC} measure
- 30kHz to 1.1MHz
- f_M divider
- Up to 1024 OSR

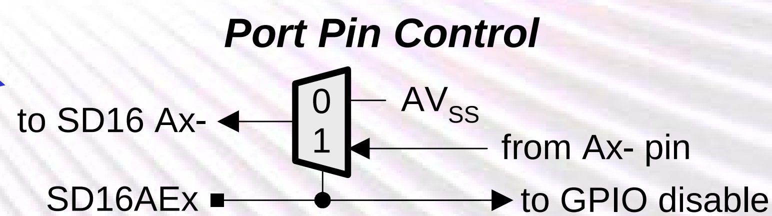


SD16_A Input Design

- **Four external input pairs**
- **Fully differential**
- **Internal channels:**
  - Temperature
  - AV_{CC} / 11
  - Offset shunt
- **Selectable current vs. speed input buffer**
- **PGA: 1, 2, 4, 8, 16 & 32x**



- **SD16AEx bits for internal A_{IN}- connection to AV_{SS}**



**** Buffer not in 'F20x3 devices***

Input Select vs. Channel Select

- **SD16_A: 1 channel, 4 external inputs per channel**
  - MSP430F42x0 & MSP430F20x3
- **SD16: 3 channels, 1 external input per channel**
  - MSP430FE42x & MSP430F42x
- **Channels are independent & can operate in parallel**
- **Inputs are multiplexed into each channel & must be selected/sampled sequentially**

SD16 Conversion Modes

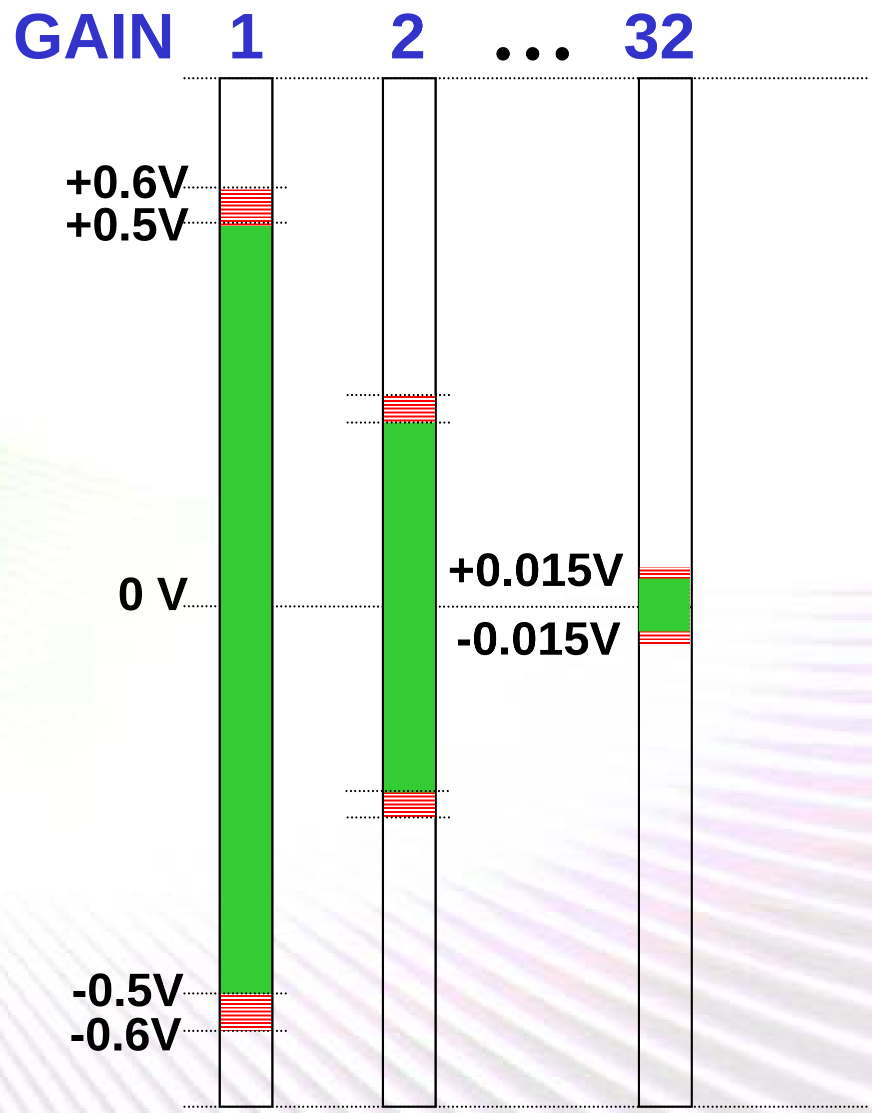
Mode	Operation
Single Channel, Single Conversion	**A single channel is converted once.**
Single Channel, Continuous Conversion	**A single channel is converted continuously.**
Group of Channels, Single Conversion (SD16 only)	**A group of channels is converted once.**
Group of Channels, Continuous conversion (SD16 only)	**A group of channels is converted continuously.**

Analog Input Range

- What is V_{REF}?
- What is the PGA setting?

$$V_{FSR} = \frac{V_{ref} / 2}{GAIN_{PGA}}$$

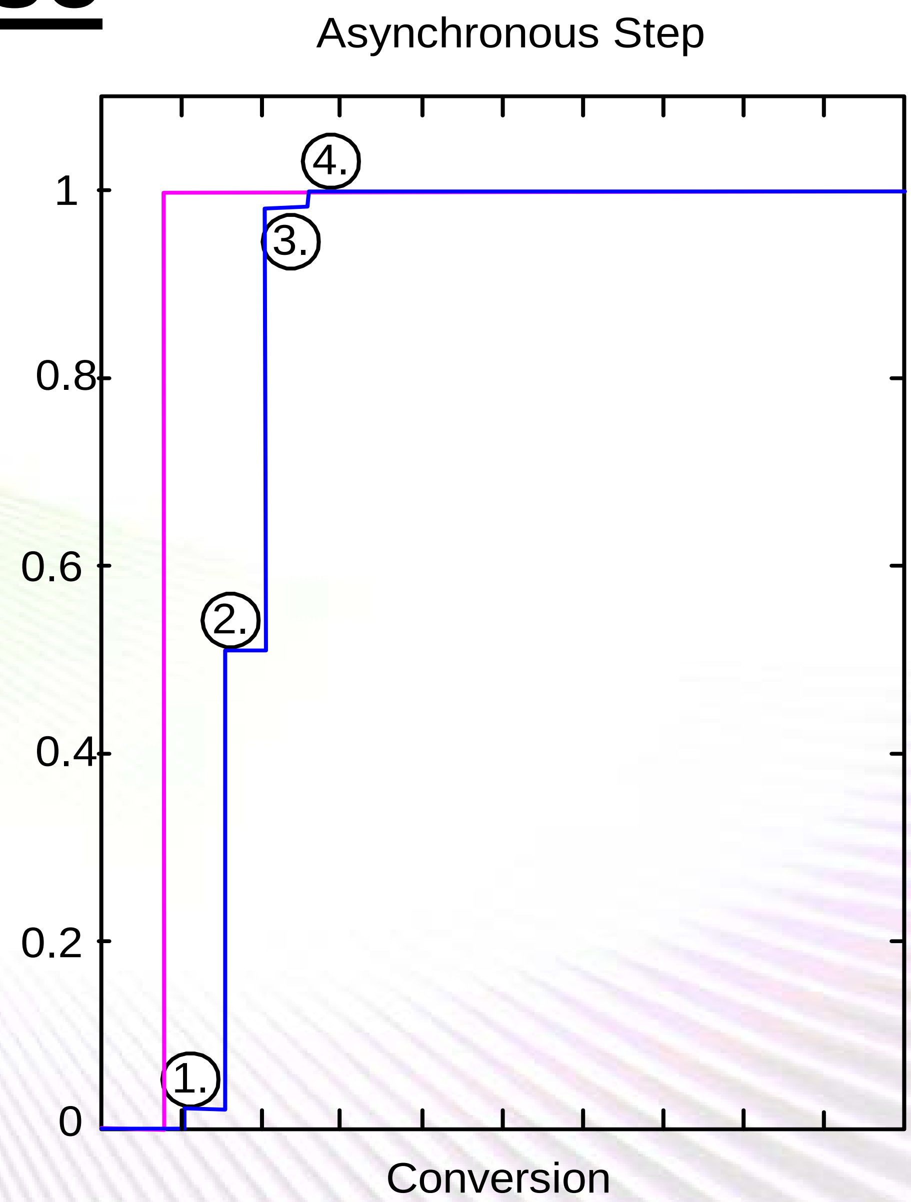
- Applies to all inputs & modes



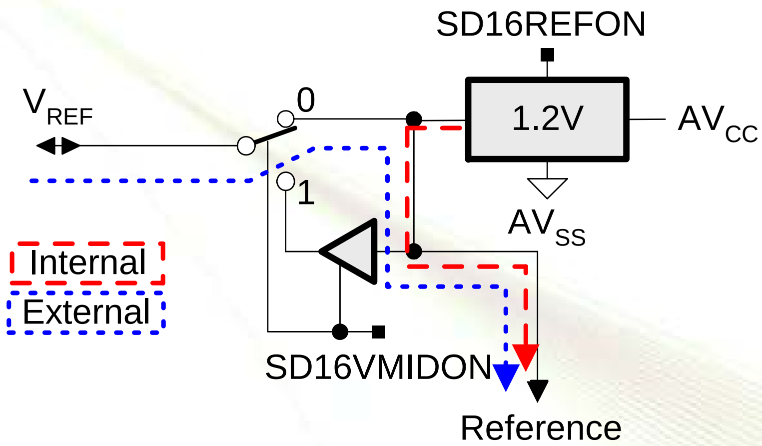
** 0V = Vss (SD16), 0V = relative (SD16A)*

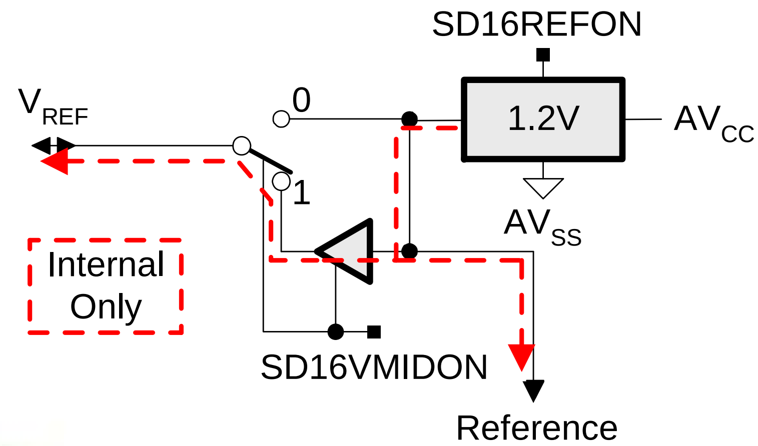
Input Step Response

- **Key for mux switching**
- **Decimation filter must cycle out the delta**
- **SD16INTDLYx sets automatic settling time to 1st conversion interrupt**
- **f_M = 1.048MHz; OSR = 256**
  - f_{SAMPLE} = 4.096 ksps ->
  - $t_{SETTLE(MAX)}$ ~ 732usec



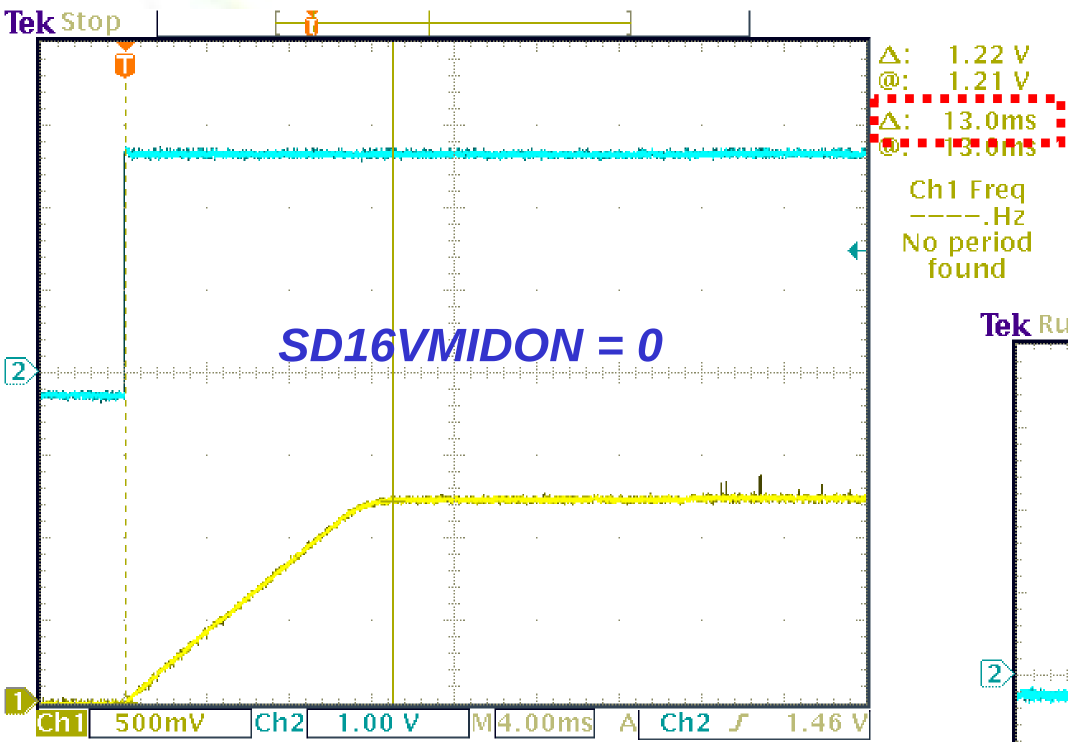
Internal Reference

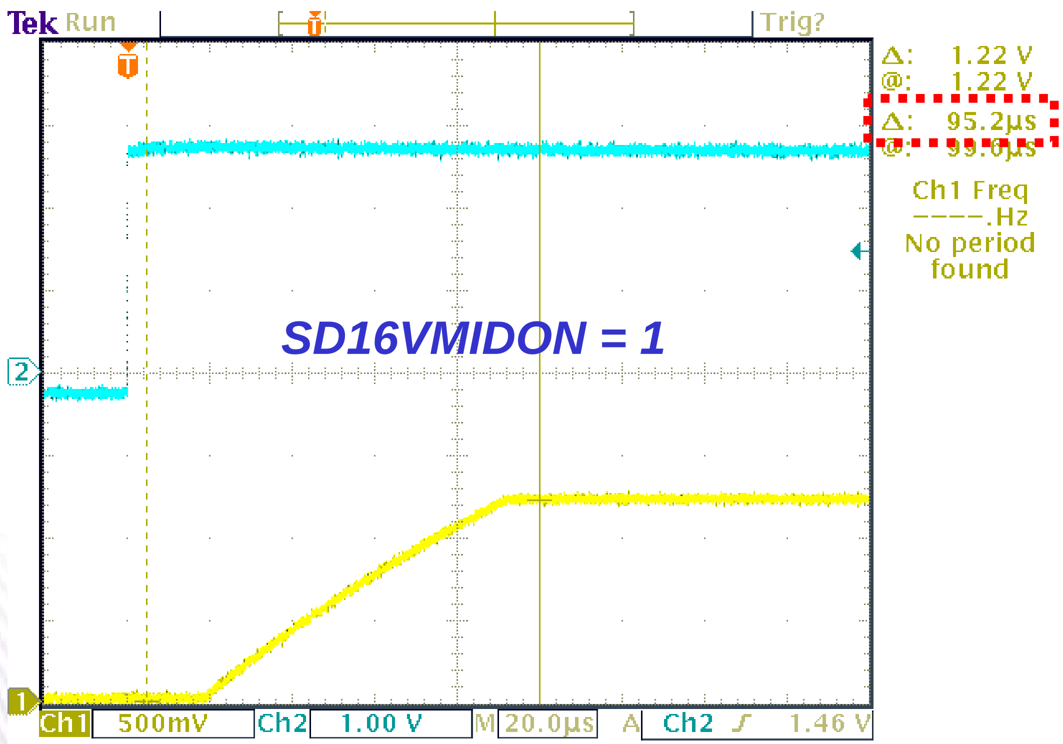




- **Internal 1.2V reference**
- **20ppm temperature coefficient**
- **V_{REF} Options:**
  - External ref: SD16REFON = 0, SD16VMIDON = 0
  - Internal ref: SD16REFON = 1, SD16VMIDON = 0
  - Internal ref w/ buffered output: SD16REFON = 1, SD16VMIDON = 1
- **For temperature (A6): use internal reference**

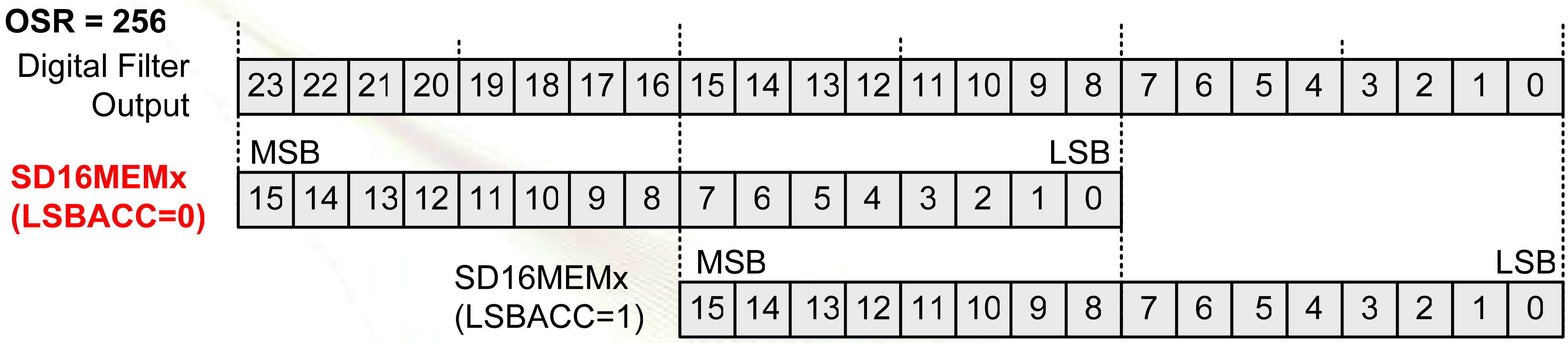
Internal Reference Settling Time





- C_{VREF} = 470nF
- Ref buffer = +100x faster reference settling
- Disable once settled

SD16 Data



- Normal mode reads 16-bit
- 24-bit access available

Agenda

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ADC Lab – Goal

- Use ADC12 integrated temperature sensor
- Setup ADC12 to perform single conversion
- Loop continuously, converting to Degrees F and C in software
- Touch the MSP430 with finger to change temperature

ADC Lab - Considerations

- What must be set to make the ADC work?
- Sampling Time
- Input Clock
- Trigger
- Input Channel
- Mode

ADC Lab – Code

```
ADC12CTL0 = _________________________________;
// Setup ADC12, ref., sampling time
ADC12CTL1 = ___;      // Use sampling timer
ADC12MCTL0 = _____________; // Select channel A10, Vref+
ADC12IE = 0x01;       // Enable ADC12IFG.0
for (i = 0; i < 0x3600; i++); // Delay for reference start
ADC12CTL0 |= ENC;     // Enable conversions
__enable_interrupt();// Enable interrupts

while(1)
{
  ADC12CTL0 |= _______; // Start conversion
```

ADC Lab – Sampling Time

- **Check Device Datasheet**

$t_{SENSOR(sample)}$	Sample time required if channel 10 is selected (see Note 3)	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V	30	µs
			3 V	30	

- **Available clocks:**
  - ACLK (32.768 kHz)
  - SMCLK (1MHz)
  - ADC internal OSC:

$f_{ADC12OSC}$	Internal ADC12 oscillator	ADC12DIV=0, $f_{ADC12CLK}=f_{ADC12OSC}$	V_{CC} = 2.2 V/ 3 V	3.7	5	6.3	MHz

30us with a 6 MHz clock = 189 clocks

ADC Lab – Reference

- **ADC12 has a built in reference generator that is selectable to be 1.5V or 2.5V**
- **ADC12 can also accept an external reference on the Veref+/Veref- pins**
- **ADC12 can select Vcc as a reference**

ADC Lab Setting the bits

SHT0x	Bits 11-8	Sample-and-hold time. These bits define the number of ADC12CLK cycles in the sampling period for registers ADC12MEM0 to ADC12MEM7.

SHTx Bits	ADC12CLK cycles
0111	192

REF2_5V	Bit 6	Reference generator voltage. REFON must also be set. 0 1.5 V 1 2.5 V
REFON	Bit 5	Reference generator on 0 Reference off 1 Reference on
ADC12ON	Bit 4	ADC12 on 0 ADC12 off 1 ADC12 on

```
ADC12CTL0 = ADC12ON + REFON + REF2_5V + SHT0_7;
```

SHP	Bit 9	Sample-and-hold pulse-mode select. This bit selects the source of the sampling signal (SAMPCON) to be either the output of the sampling timer or the sample-input signal directly.

```
ADC12CTL1 = SHP;
```

ADC Lab - Defaults

- **ADC12CTL1**

SHSx	Bits 11-10	Sample-and-hold source select	
		00	ADC12SC bit
		01	Timer_A.OUT1
		10	Timer_B.OUT0
		11	Timer_B.OUT1
ADC12 SSELx	Bits 4-3	ADC12 clock source select	
		00	ADC12OSC
		01	ACLK
		10	MCLK
		11	SMCLK
CONSEQx	Bits 2-1	Conversion sequence mode select	
		00	Single-channel, single-conversion
		01	Sequence-of-channels
		10	Repeat-single-channel
		11	Repeat-sequence-of-channels

ADC Lab – Configuring the conversion

SREFx	Bits 6-4	Select reference 000 $V_{R+} = AV_{CC}$ and $V_{R-} = AV_{SS}$ 001 $V_{R+} = V_{REF+}$ and $V_{R-} = AV_{SS}$ 010 $V_{R+} = Ve_{REF+}$ and $V_{R-} = AV_{SS}$ 011 $V_{R+} = Ve_{REF+}$ and $V_{R-} = AV_{SS}$ 100 $V_{R+} = AV_{CC}$ and $V_{R-} = V_{REF-}/ Ve_{REF-}$ 101 $V_{R+} = V_{REF+}$ and $V_{R-} = V_{REF-}/ Ve_{REF-}$ 110 $V_{R+} = Ve_{REF+}$ and $V_{R-} = V_{REF-}/ Ve_{REF-}$ 111 $V_{R+} = Ve_{REF+}$ and $V_{R-} = V_{REF-}/ Ve_{REF-}$
INCHx	Bits 3-0	Input channel select 0000 A0 0001 A1 0010 A2 0011 A3 0100 A4 0101 A5 0110 A6 0111 A7 1000 Ve_{REF+} 1001 V_{REF-}/Ve_{REF-} 1010 Temperature sensor

```
ADC12MCTL0 = INCH_10 + SREF_1;
```

ADC Lab – Final code

```
ADC12CTL0 = ADC12ON + REFON + REF2_5V + SHT0_7;
// Setup ADC12, ref., sampling time
 ADC12CTL1 = SHP;      // Use sampling timer
 ADC12MCTL0 = INCH_10 + SREF_1; // Select channel A10, Vref+
 ADC12IE = 0x01;       // Enable ADC12IFG.0
 for (i = 0; i < 0x3600; i++); // Delay for reference start
 ADC12CTL0 |= ENC;     // Enable conversions
 __enable_interrupt();// Enable interrupts

 while(1)
 {
   ADC12CTL0 |= ADC12SC; // Start conversion
```

Agenda

- Analog measurements with the MSP430
  - **Comparator, ADC10, ADC12, SD16, SD16_A**
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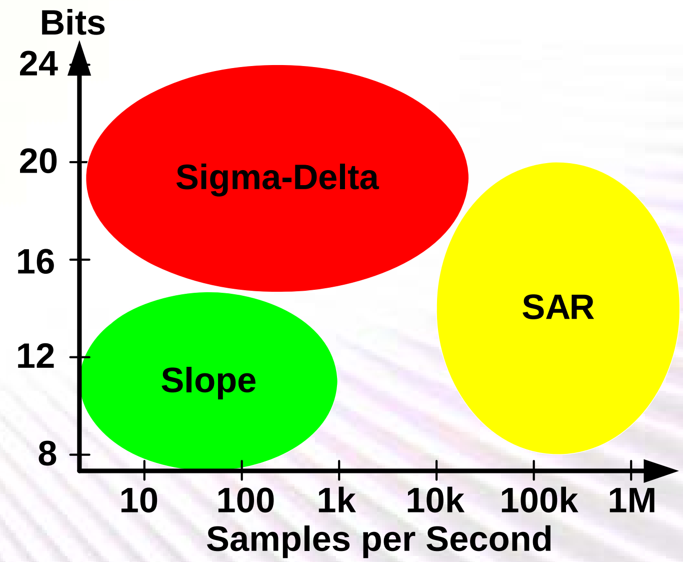
Selecting an MSP430 ADC

	channels	f SAMPLE (ksps)		res	SINAD (typ)	A IN	reference			triggering	gain	features
		min	max				Ref IN	Ref OUT	Ref I_OUT			
ADC10	8	34	200+	10	57	Vss to Vref	1.4-3.6	1.5/2.5V	+/-1mA	SW/Timer/Cont	N/A	DTC
ADC12	12	34	200+	12	68	Vss to Vref	1.4-3.6	1.5/2.5V	+/-1mA	SW/Timer/Cont	N/A	Conv Mem
SD16	3 ind	~4		16	85	+/-600mV	1.0-1.5	1.2V	+/-1mA	SW/Cont	to 32x	Preload
SD16_A	4 mux'd	~0.03	~5	16	85	+/-600mV	1.0-1.5	1.2V	+/-1mA	SW/Cont	to 32x	Buffered input

- **Voltage range to be measured?**
- **Max frequency for A_{IN}?**
- **How much resolution?**
- **Differential inputs?**
- **Reference range?**
- **Multiple channels?**



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