MSP430F2xx Family Enhancements and Features

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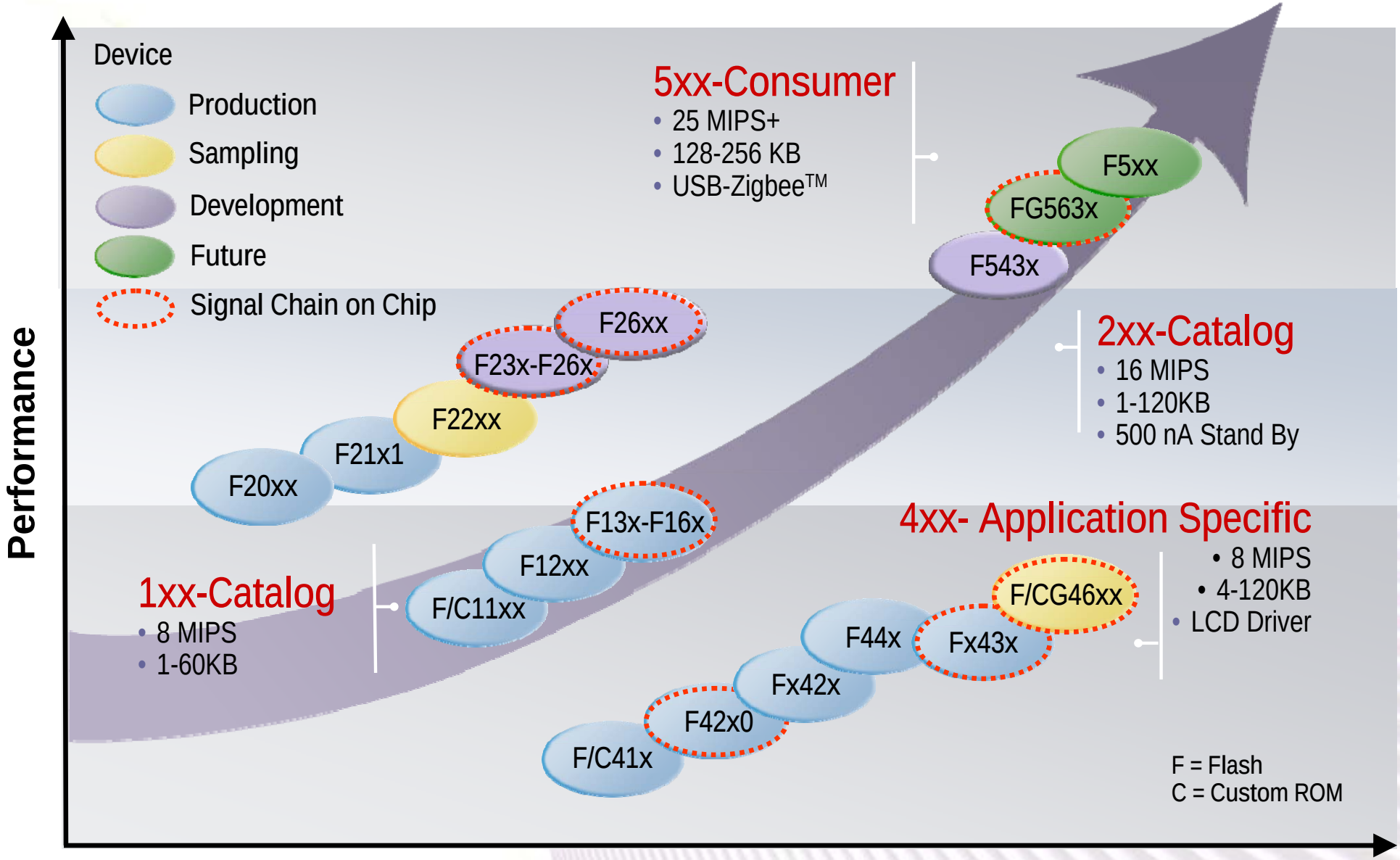
Agenda

- Enhancements
- Application Examples
- Devices & Summary

MSP430 Products



MSP430F2xx – What's Different

- *Faster*
- *Lower power*
- *New peripherals*
- Compatible migration path with the '1xx
- Great starting point for new applications
- Complete family of new devices planned

MSP430F1xx Versus MSP430F2xx

	1xx	2xx
CPU Clock	8MHz	16MHz
Wakeup	6us	1us
Stand-by	<2uA	<1uA
BOR	Some	ALL
Flash ISP	2.7V	2.2V
P1/2	-	Pull-up / Down
Oscillator	±20%	±2.5%
OscFault	HF	HF/LF
Watchdog	SW	SW Invalid Address Clock Fault
BSL	2^256	Hackproof

2X faster

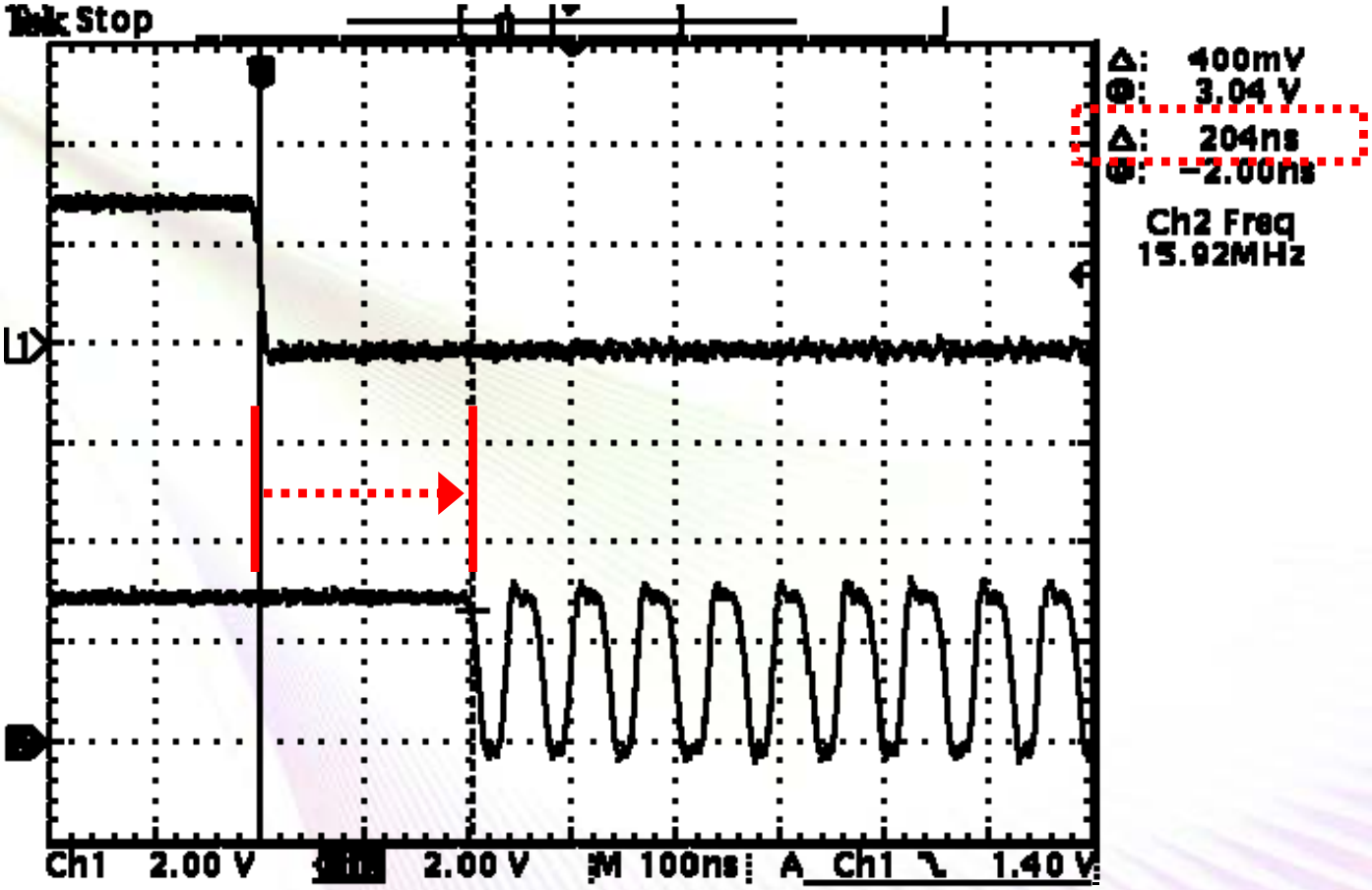
1/2 power

Improved

F2xx 16MIPS On-Demand

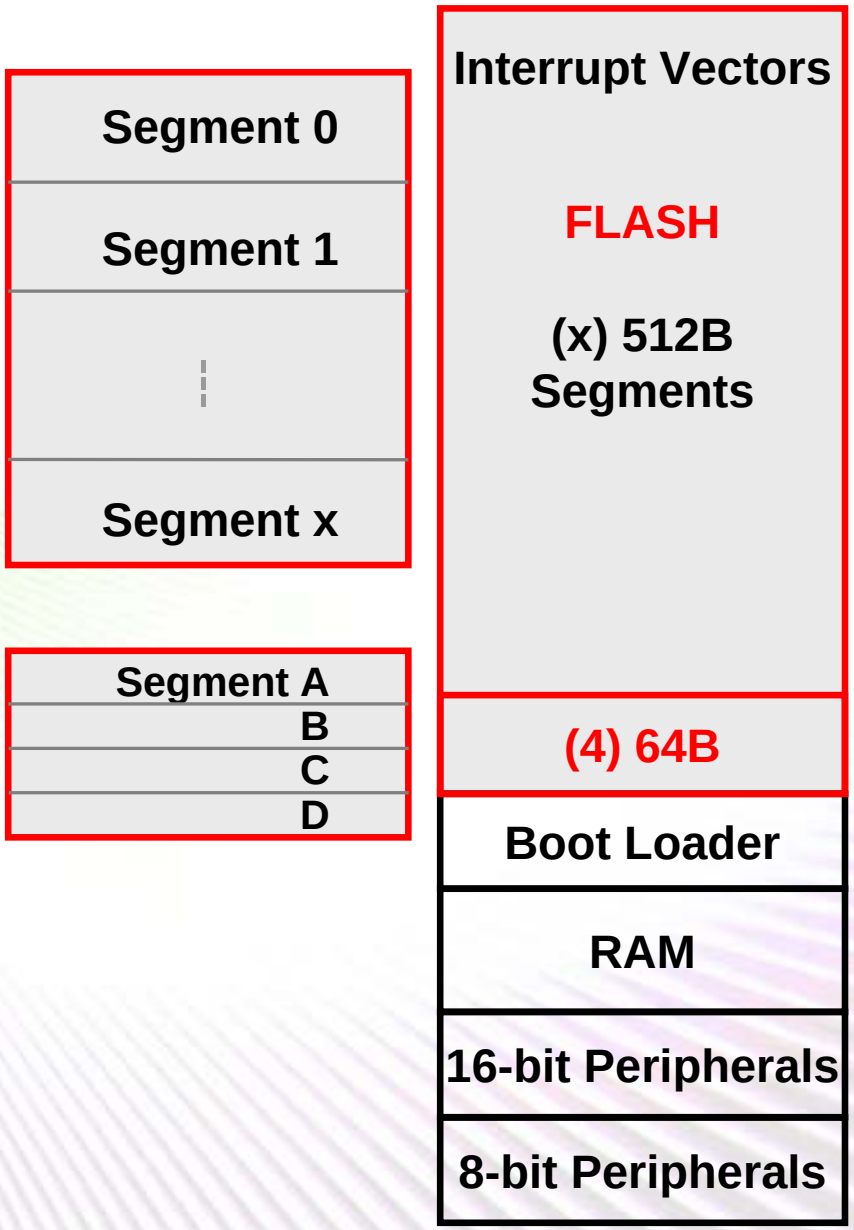
Interrupt

Oscillator

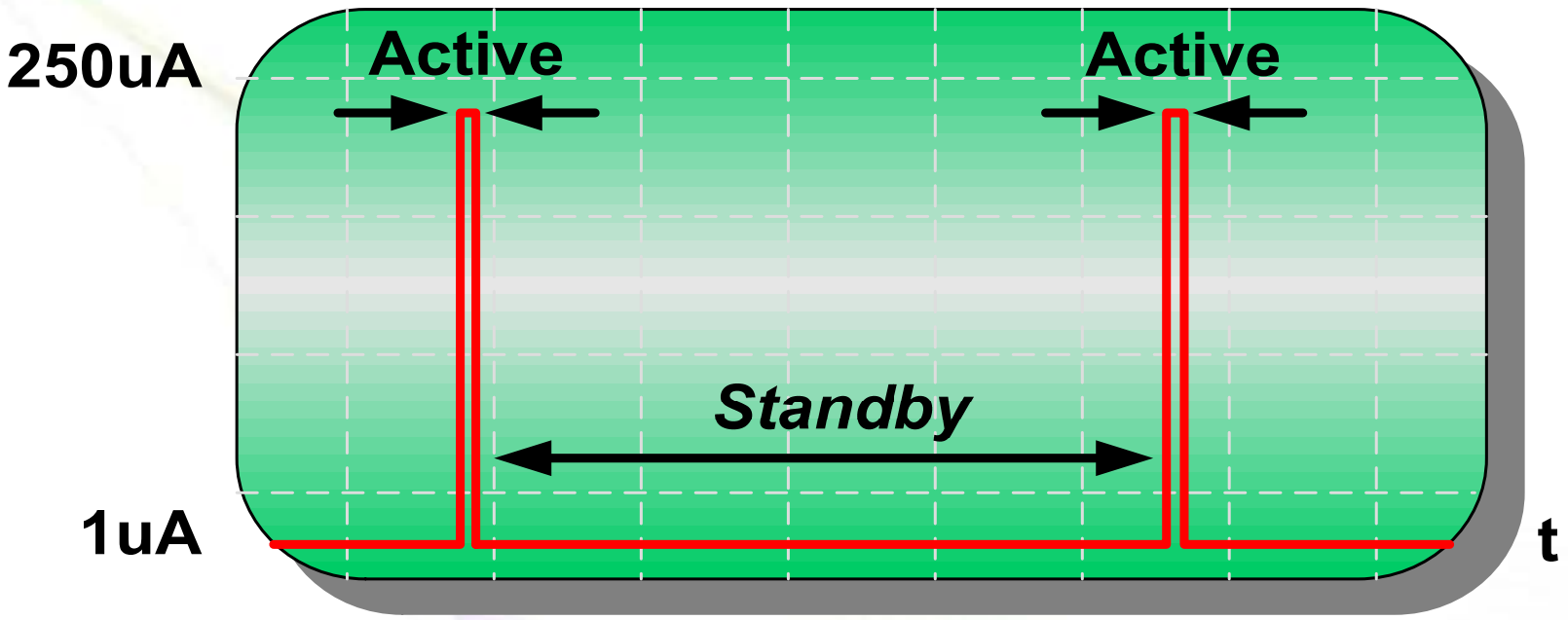


F2xx Flash

- Fast <20us /byte ISP
- ISP down to 2.2V
- Interruptible ISP/Erase
- Reduced size 64B info memory segments
- Lock(able) info segment A
- Improved BSL security
- Protection against program/erase from accidental BSL entry



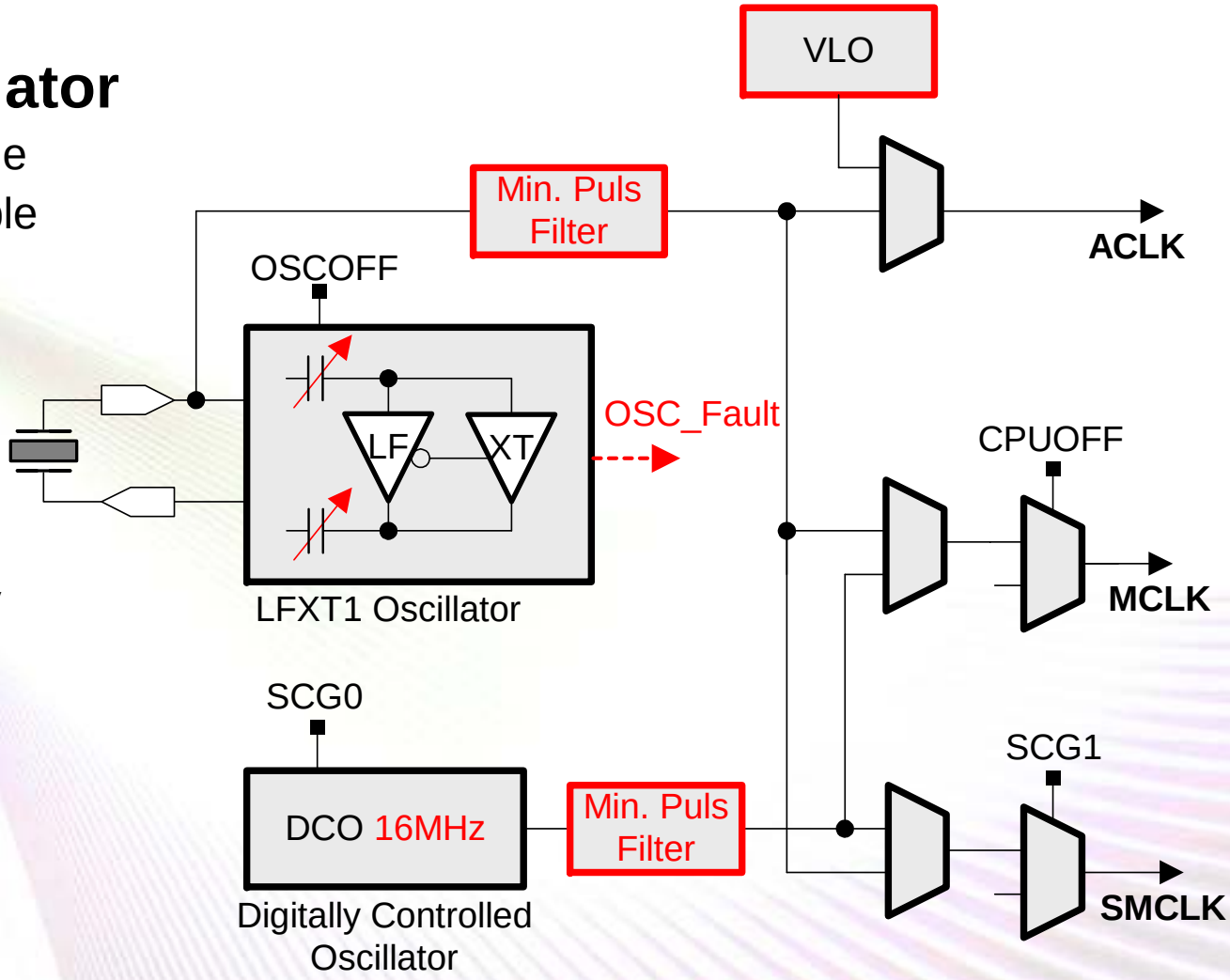
Achieving *Ultra-low Power*



- Max time in Ultra-low Power *LPM3* standby mode
- *Active* Performance on-demand
- Minimum active duty cycle

F2xx Basic Clock+

- **LFXT1 XTAL Oscillator**
  - <1uA LPM3 standby mode
  - XTAL CAPs programmable
  - OSCfault LF/(XT)
  - New VLO
- **Improved DCO**
  - < 1us 0-to-16MHz
  - ± 2.5% DCO
  - Programmable frequency
- **VLO not in ’21x1**



F2xx: No XTAL Required – DCO+

calibrated DCO frequencies − tolerance at calibration

PARAMETER	TEST CONDITIONS	T_A	VCC	MIN	TYP	MAX	UNIT
Frequency tolerance at calibration		25°C	3 V	−1	±0.2	+1	%

calibrated DCO frequencies − tolerance over temperature 0°C − +85°C

PARAMETER	TEST CONDITIONS	T_A	VCC	MIN	TYP	MAX	UNIT
1 MHz tolerance over temperature		0–85°C	3.0 V	−2.5	±0.5	+2.5	%
8 MHz tolerance over temperature		0–85°C	3.0 V	−2.5	±1.0	+2.5	%
12 MHz tolerance over temperature		0–85°C	3.0 V	−2.5	±1.0	+2.5	%
16 MHz tolerance over temperature		0–85°C	3.0 V	−3.0	±2.0	+3.0	%

calibrated DCO frequencies − tolerance over supply voltage V_{CC}

PARAMETER	TEST CONDITIONS	T_A	VCC	MIN	TYP	MAX	UNIT
1 MHz tolerance over V_{CC}		25°C	1.8 V – 3.6 V	−3	±2	+3	%
8 MHz tolerance over V_{CC}		25°C	1.8 V – 3.6 V	−3	±2	+3	%
12 MHz tolerance over V_{CC}		25°C	2.2 V – 3.6 V	−3	±2	+3	%
16 MHz tolerance over V_{CC}		25°C	3.0 V – 3.6 V	−3	±2	+3	%

calibrated DCO frequencies − overall tolerance

PARAMETER	TEST CONDITIONS	T_A	VCC	MIN	TYP	MAX	UNIT
1 MHz tolerance overall		I: -40–85°C T: -40–105°C	1.8 V – 3.6 V	−5	±2	+5	%
8 MHz tolerance overall		I: -40–85°C T: -40–105°C	1.8 V – 3.6 V	−5	±2	+5	%
12 MHz tolerance overall		I: -40–85°C T: -40–105°C	2.2 V – 3.6 V	−5	±2	+5	%
16 MHz tolerance overall		I: -40–85°C T: -40–105°C	3.0 V – 3.6 V	−6	±3	+6	%

Loading DCO Calibration Data

DCO Calibration Data (provided from factory in flash info memory segment A)			
DCO Frequency	Calibration Register	Size	Address
1 MHz	CALBC1_1MHz	byte	010FFh
	CALDCO_1MHz	byte	010FEh
8 MHz	CALBC1_8MHz	byte	010FDh
	CALDCO_8MHz	byte	010FCh
12 MHz	CALBC1_12MHz	byte	010FBh
	CALDCO_12MHz	byte	010FAh
16 MHz	CALBC1_16MHz	byte	010F9h
	CALDCO_16MHz	byte	010F8h

```
BCSCTL1 = CALBC1_16MHZ;          // DCO = 16MHz
DCOCTL = CALDCO_16MHZ;
```

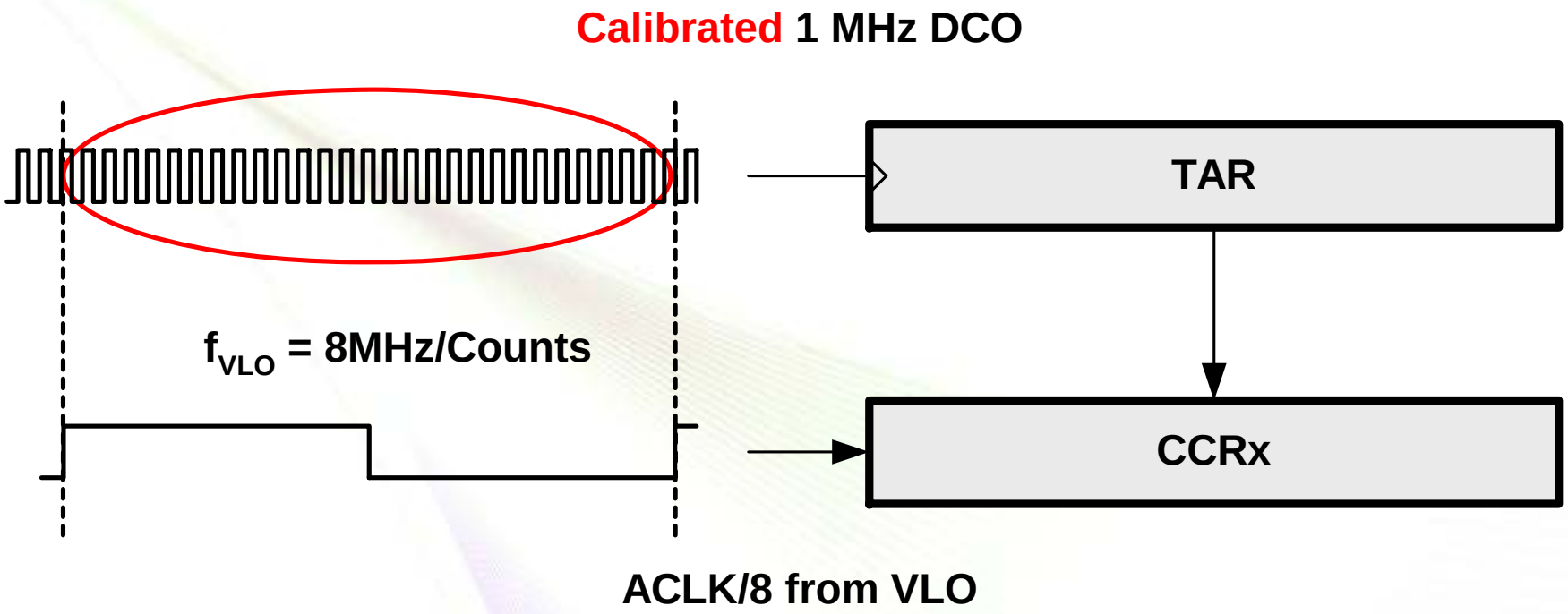
VLO Specs

internal very low power, low frequency oscillator (VLO)

PARAMETER		TEST CONDITIONS	T_A	VCC	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency		-40–85°C	2.2 V/3 V	4	12	20	kHz
			105°C	2.2 V/3 V			22	
df_{VLO}/dT	VLO frequency temperature drift	(see Note 1)	I: -40–85°C T: -40–105°C	2.2 V/3 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	(see Note 2)	25°C	1.8V – 3.6V		4		%/V

- **Wide initial tolerance**
- **Temperature drift**
- **Voltage drift**
- **Calibratable, just like 1xx DCO!**

Calibrating the VLO



- Clock Timer_A from calibrated 1MHz DCO
- Capture with rising edge of ACLK/8 from VLO
- VLO = 8MHz/counts

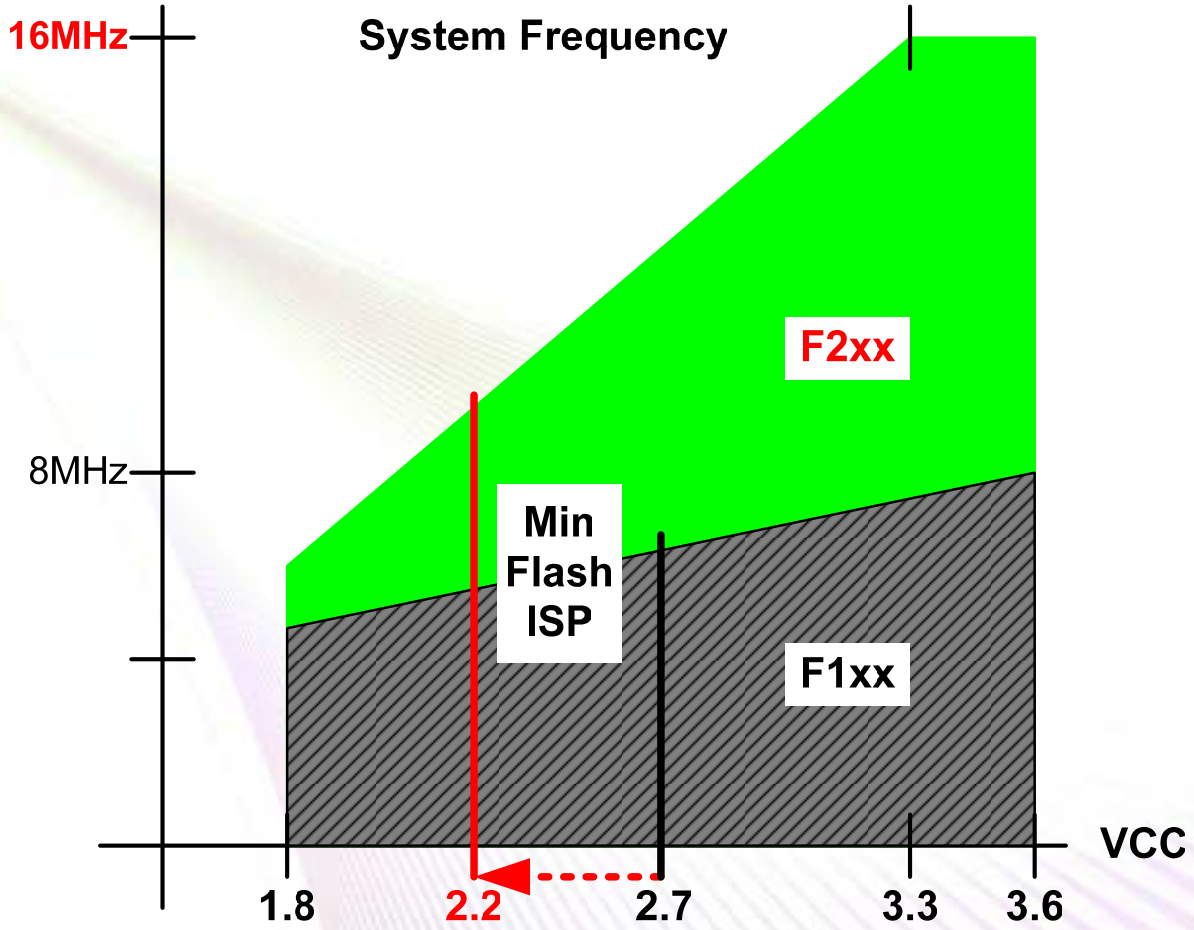
Library coming soon!

Demo: LPM3 Using VLO

```
void main(void)
{
  BCSTL3 |= LFXT1S_2;              // LFXT1 = VLO
  WDTCTL = WDT_ADLY_1000;
  IE1 |= WDTIE;
// Configure P1/P2
  for (;;){
    _BIS_SR(LPM3_bits + GIE);  // Enter LPM3
    P1OUT ^= 0x01;
  }
}
#pragma vector=WDT_VECTOR
__interrupt void watchdog_timer(void){
 _BIC_SR_IRQ(LPM3_bits);        // Clear LPM3 bits 0(SR)
}
```

- What is the measured current consumption?

F2xx Expanded Operating Range



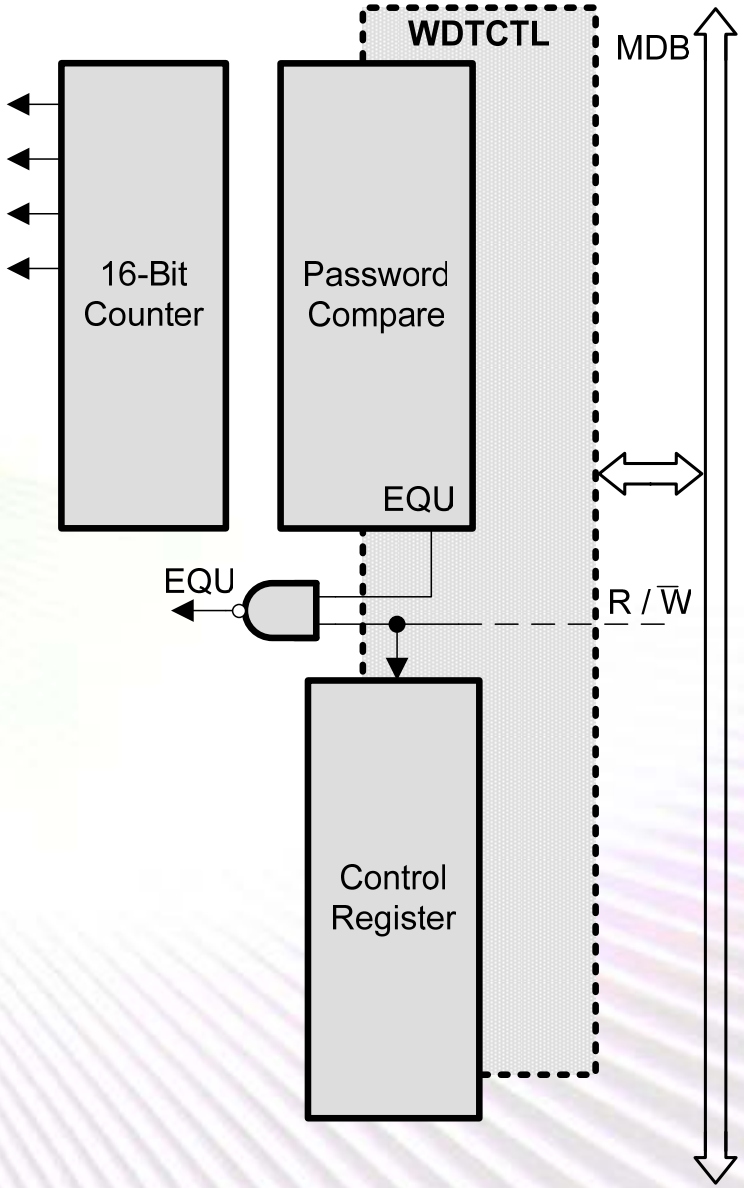
F2xx: More Robust

WDT+:

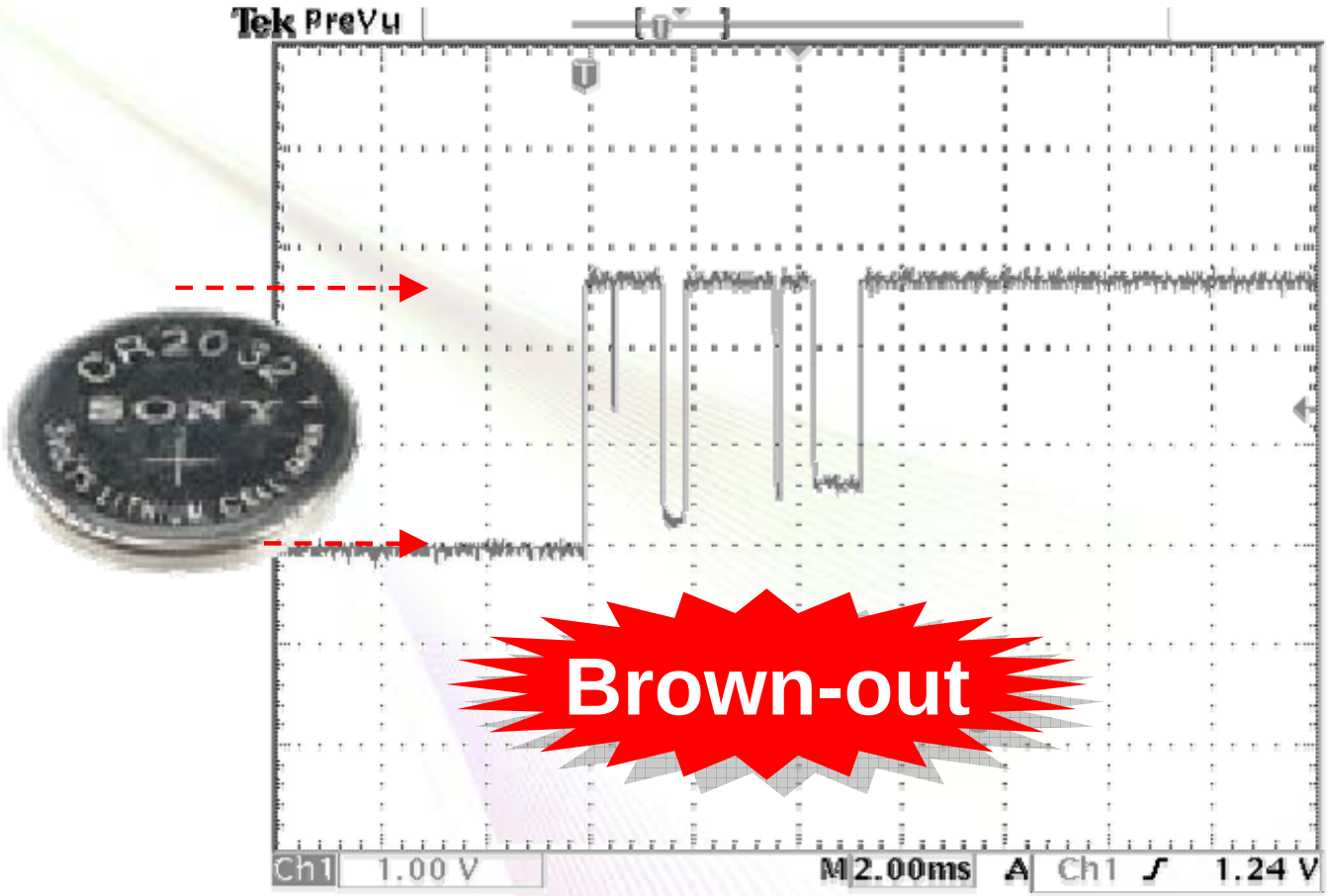
- Watchdog or interval timer
- Selectable intervals
- Password protected
- Failsafe/protected clock

System Enhancements:

- Blank device > LPM4
- Invalid address reset
- BOR on every 2xx



All F2xx Have Zero Power BOR



- **MSP430 BOR is always-on and zero-power**

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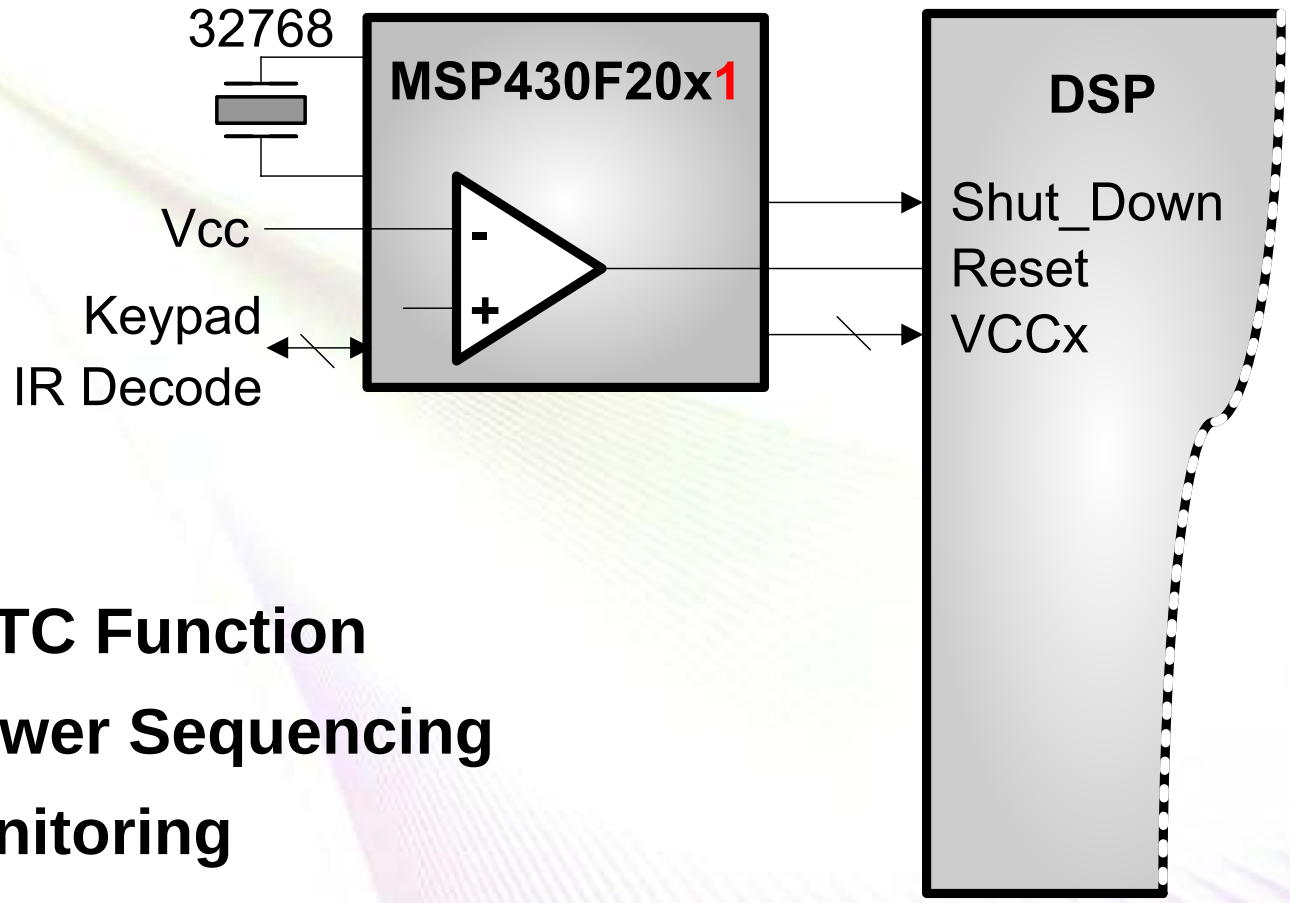
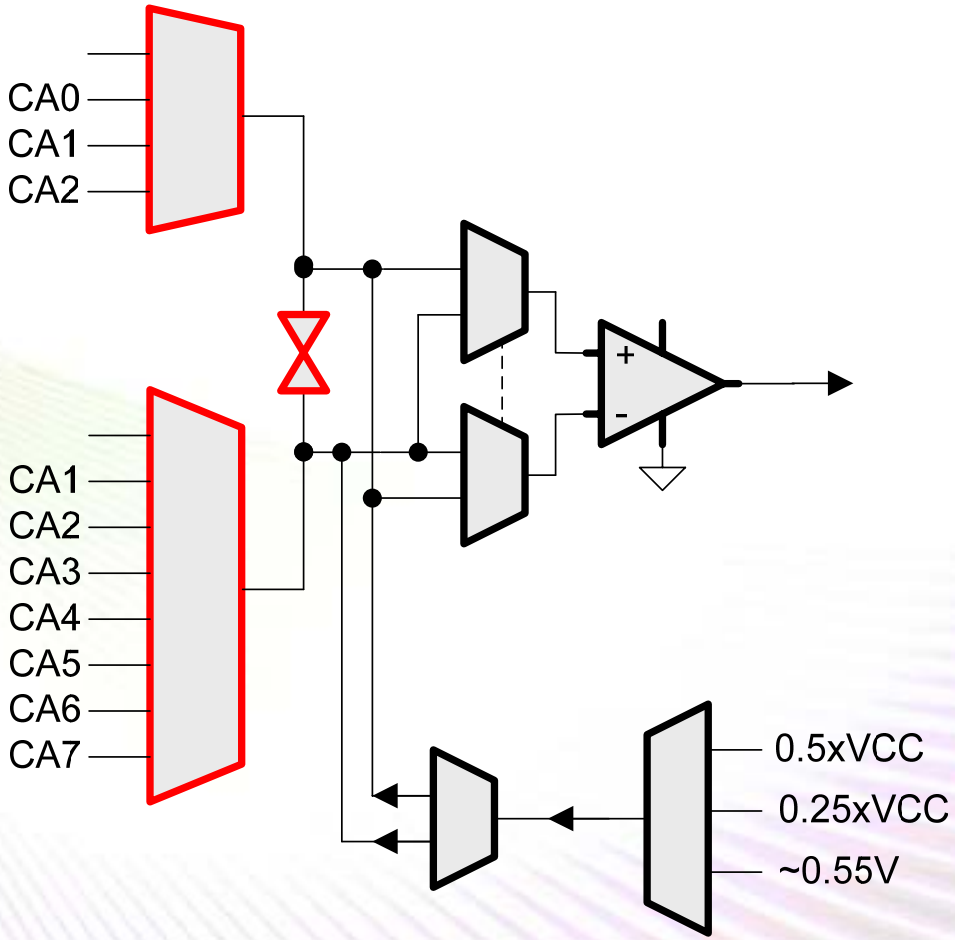
F20x1 Tiny Power Saver



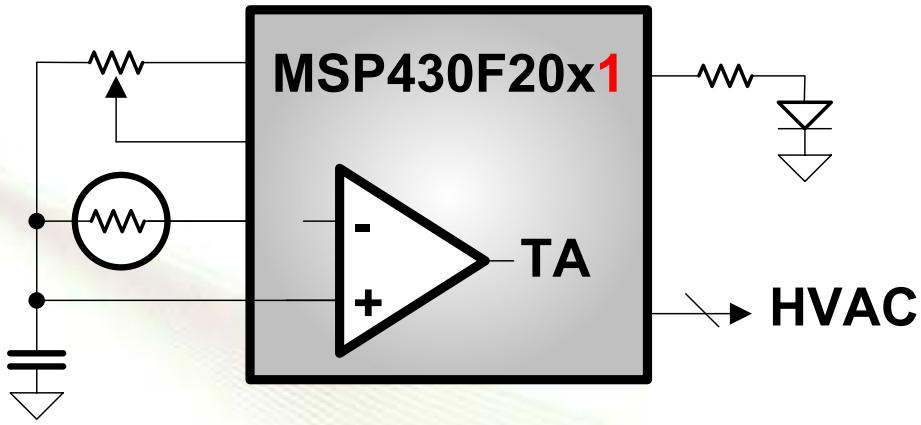
- **<1uA RTC Function**
- **DSP Power Sequencing**
- **Vcc Monitoring**
- **User Interface**
- **Tiny 4x4mm Footprint**

F2xx Comparator A+

- Slope ADC
- Battery detect
- Reference generator
- Interrupt source
- Timer_A capture
- Expanded input multiplexer
- Multiplexer short for sample-and-hold



F20x1 Residential Thermostat

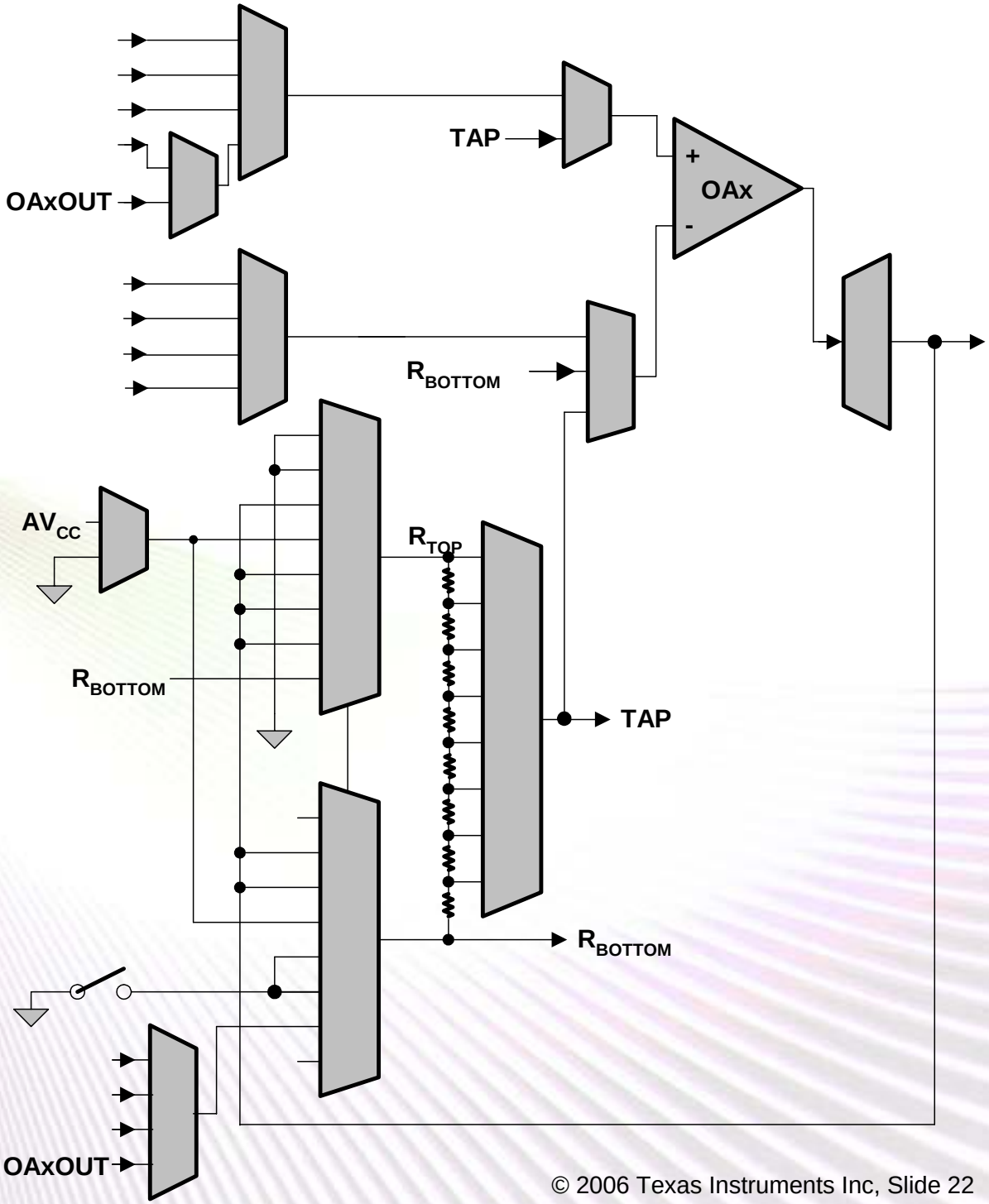


- <1uA total system power
- 10-bit slope ADC
- ± 1C/F
- No XTAL needed
- Very low cost

F2xx OA

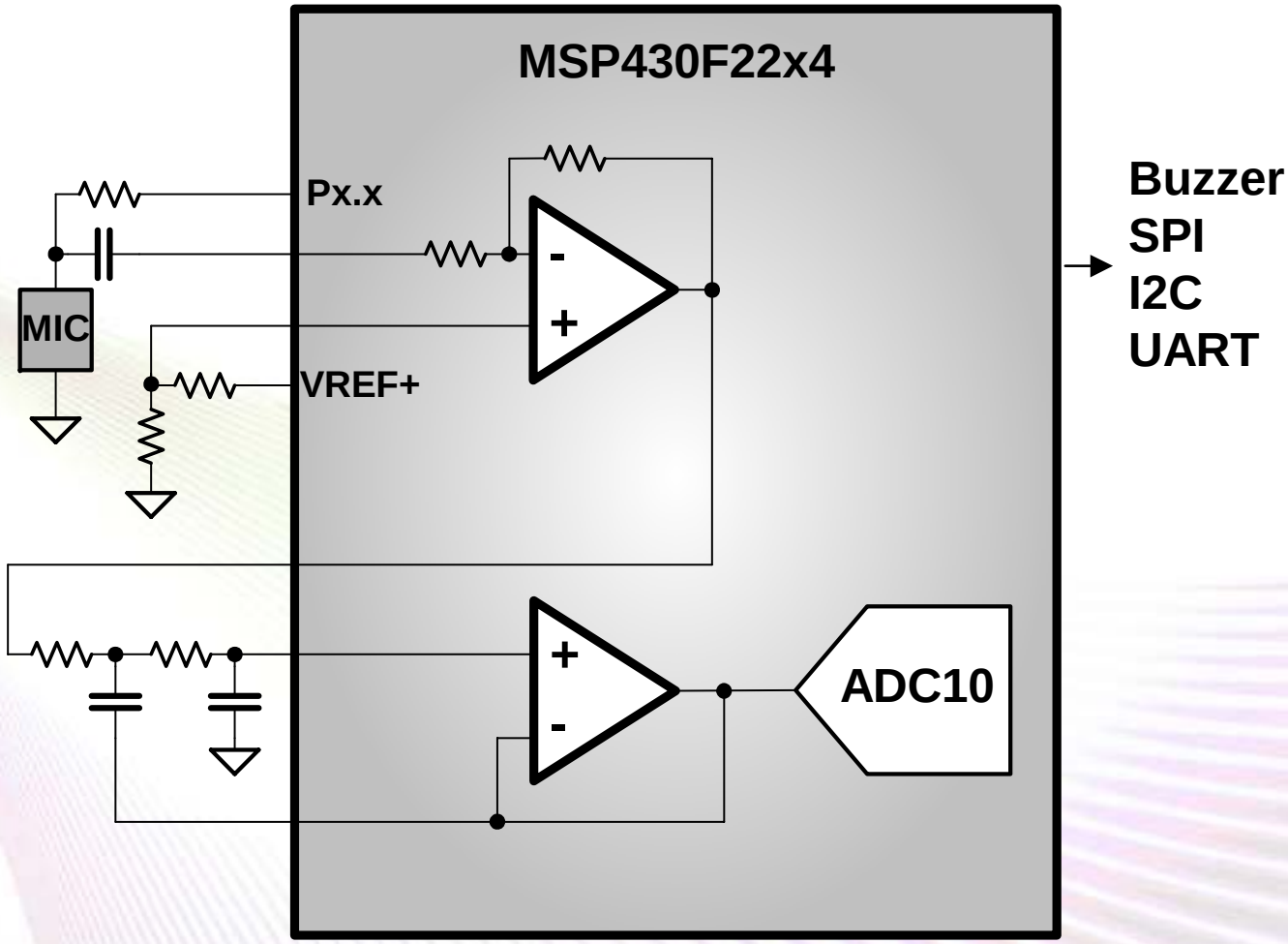
- Single-supply
- Low-current
- Rail-Rail output
- Selectable settling time vs. current consumption
- Integrated R-ladder for PGA function
- 5 modes
  - GP
  - Unity buffer
  - Comparator
  - NI PGA
  - Inverting PGA

MSP430F22x4



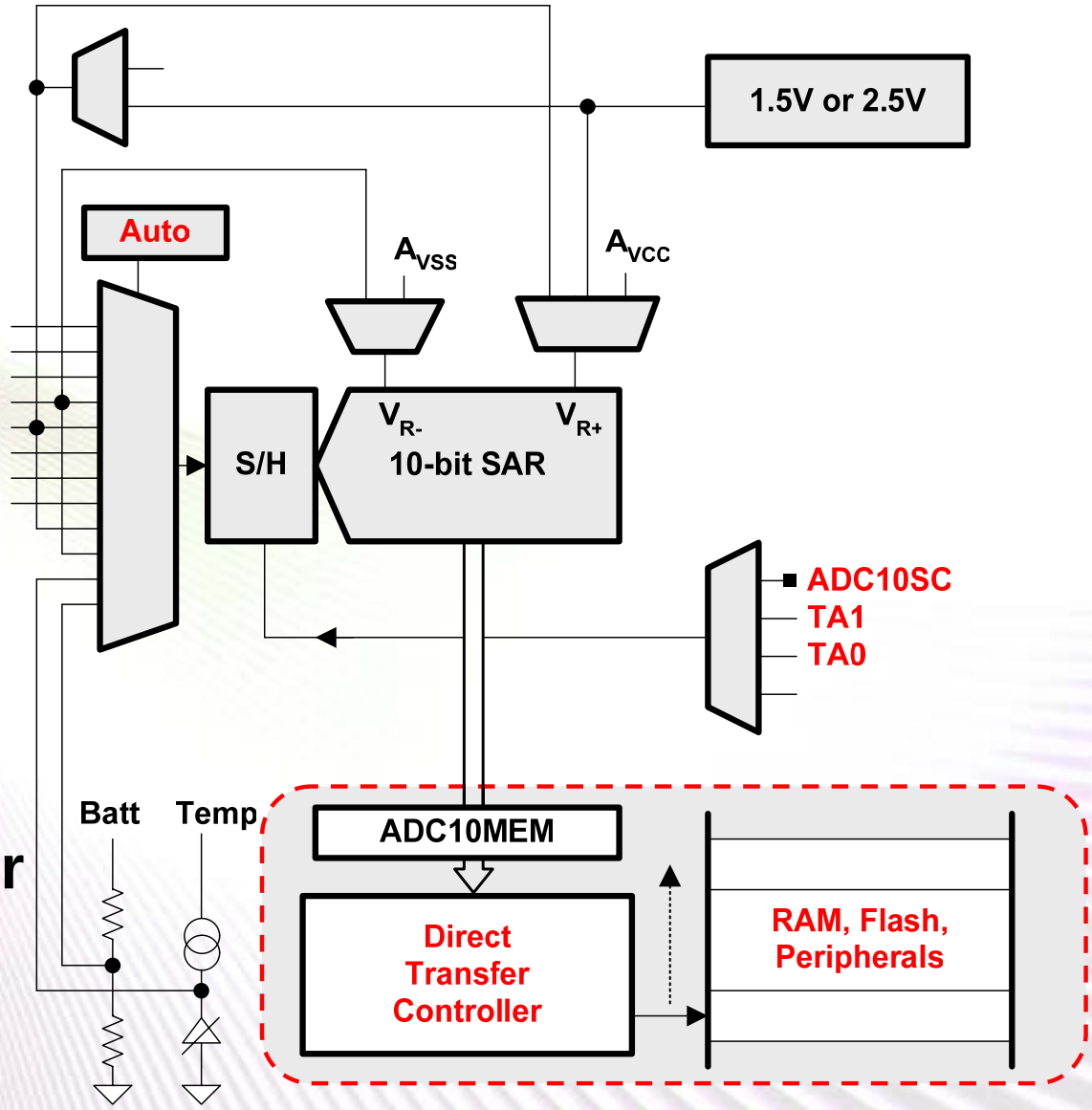
F22x4 Glass Break Detector

- Integrated Solution
- 2ms sample interval
- VLO – no crystal required
- 50uA average current
- Real-time signal analysis



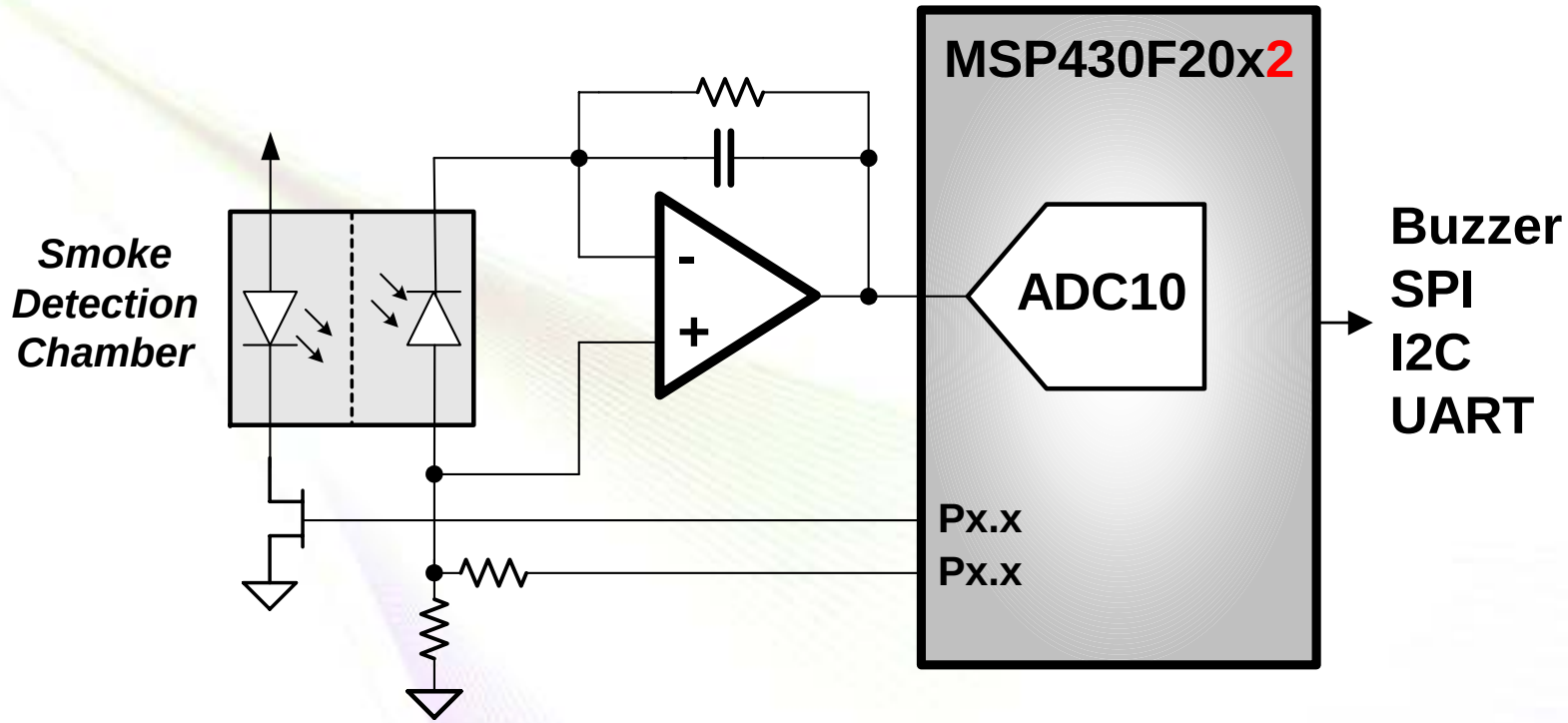
ADC10

- 10-bit ADC
- 200ksps+
- Autoscan
- Single
  Sequence
  Repeat-single
  Repeat-sequence
- Int/ext ref
- TA SOC triggers
- Data transfer controller



14-pin MSP430F2012

F20x2 Low-Cost Smoke Detector

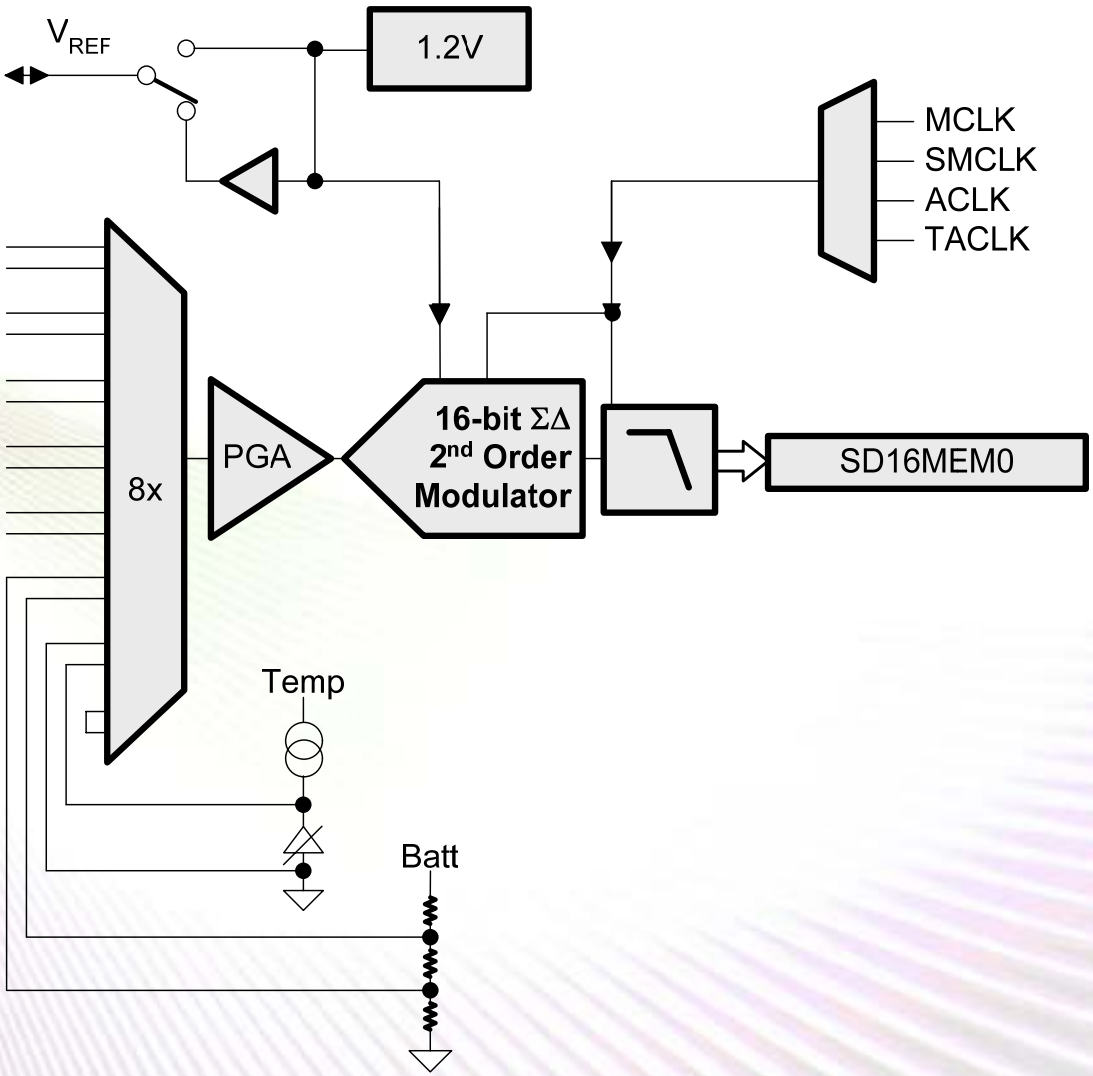


- 8s sample interval
- 2uA average system power
- VLO – no crystal required

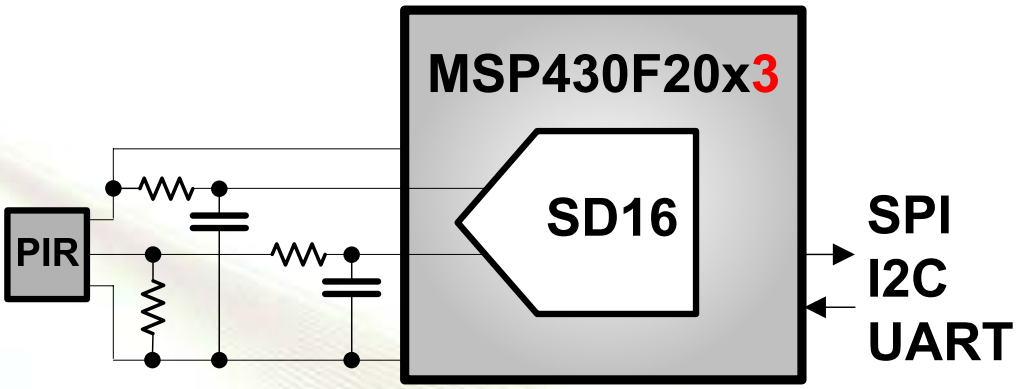
SD16_A

- 16-bit ΣΔ ADC
- 4.096 ksps
- Differential inputs
- 85db SINAD
- 32x PGA
- 18ppm 1.2V ref
- Temp sensor

14-pin MSP430F2013



F20x3 PIR Motion Detector



< 7uA total system power

- ~5uA PIR
- ~1uA Measurement
- ~0.5uA MSP430 LPM3

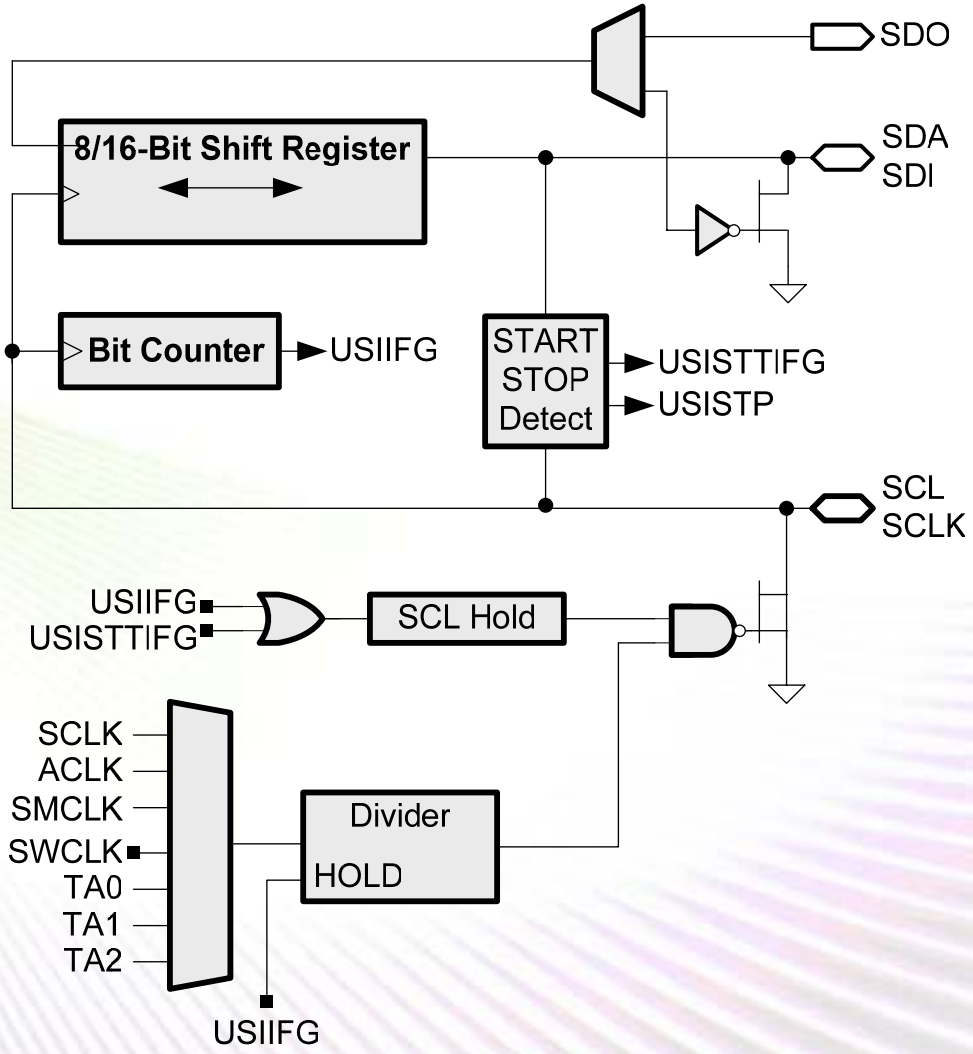
• Fully programmable

- Single-chip solution
- Direct interface to SD16
- VLO – no XTAL required

• Lower cost

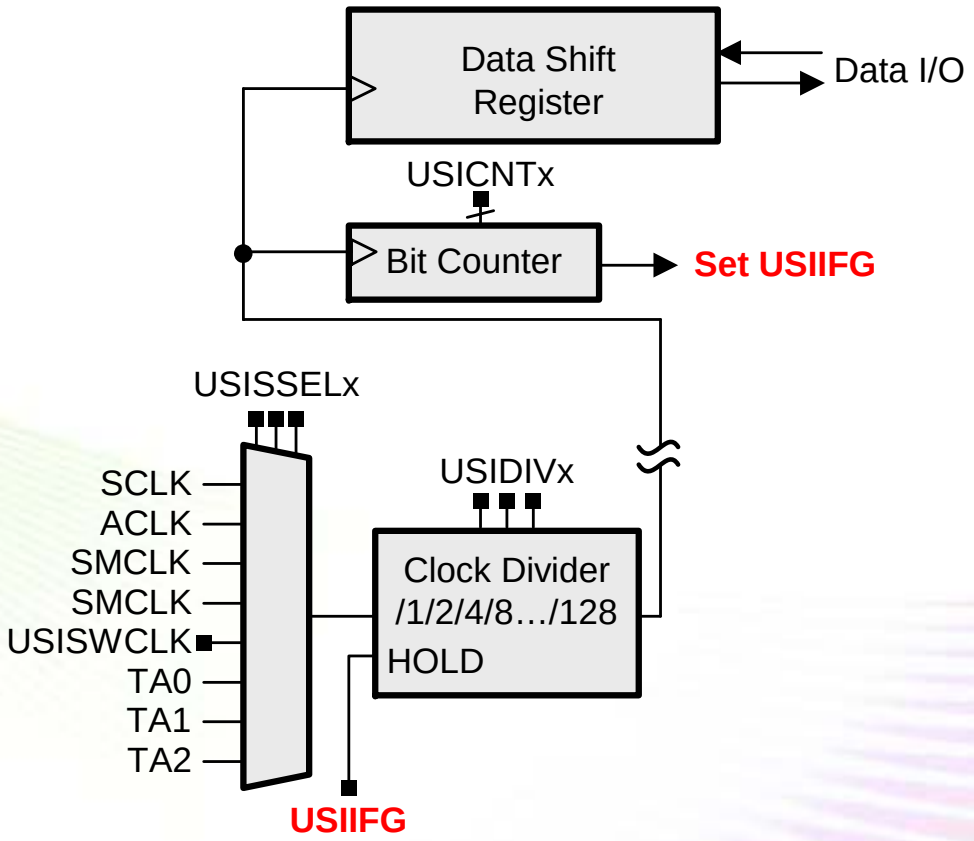
F20x2/3 Universal Serial Interface

- **Reduces CPU load**
- **SPI Mode**
  - 8/16-bit Shift Register
  - MSB/LSB first
- **I²C Mode Support**
  - START/STOP detection
  - SCL held after START
  - SCL held after counter overflow
  - Arbitration lost detection
- **Fully Static Design**
- **Interrupt Driven**

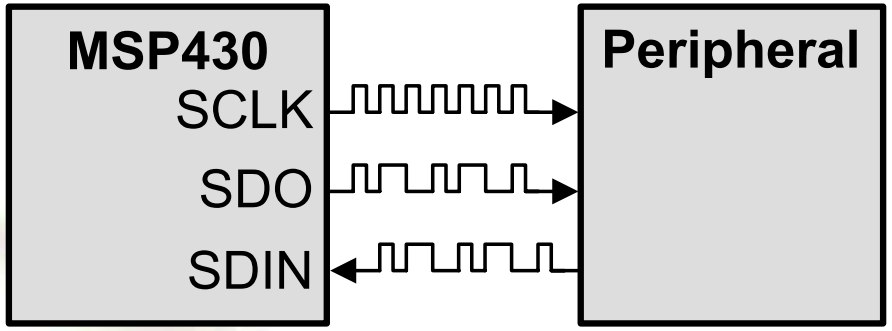


Data I/O

- Data shift register: up to 16 bits supported
- Number of bits TX'd & RX'd controlled by bit counter
- TX & RX is simultaneous
- Data I/O is user-defined: MSB or LSB first
- Bit counter automatically stops clocking after last bit & sets flag
- No data buffering!



USI Reduces CPU Load for SPI



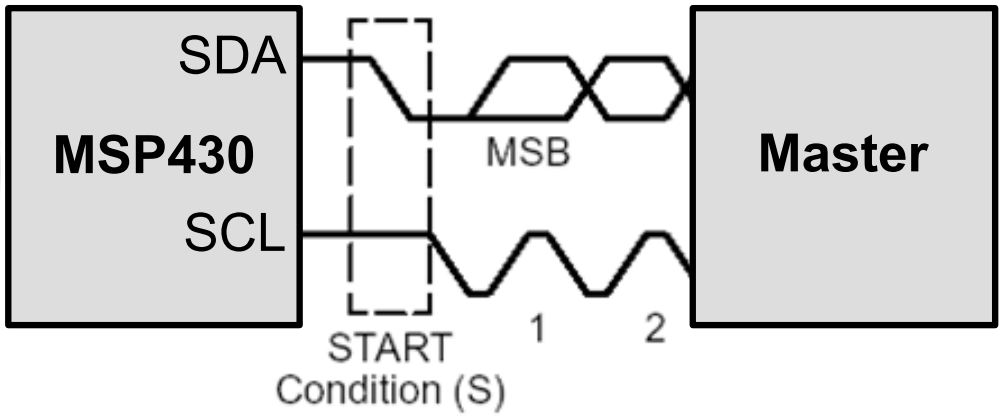

```
//Shift16_inout_Software
SR = DATA;
for (CNT=0x10;CNT>0;CNT--)
{
  P2OUT &= ~SDO;
  if (SR & 0x8000)
   P2OUT |= SDO;
  SR = SR << 1;
  if (P2IN & SDIN)
    SR |= 0x01;
  P2OUT |= SCLK;
  P2OUT &= ~SCLK;
}
```

425 Cycles

```
// Shift16_inout_USI
USISR |= DATA;
USICNT |= 0x10;
```

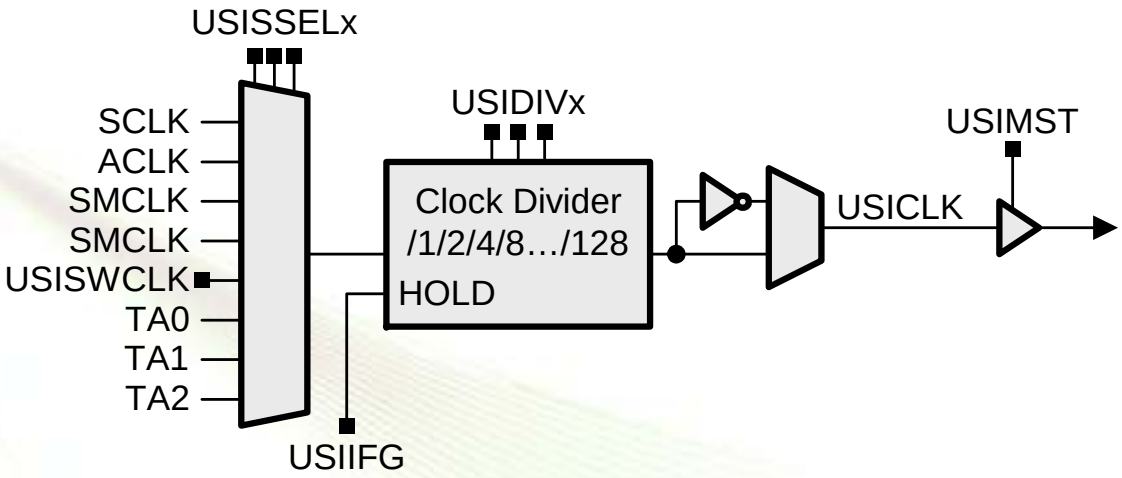
10 Cycles

F20x2/3 USI Enables Practical I2C



- I2C Slave has as little as 4us from clock edge to data
- Traditional software-only solution allows for little else
- USI hardware enables practical and compliant I2C
- Code examples on the web

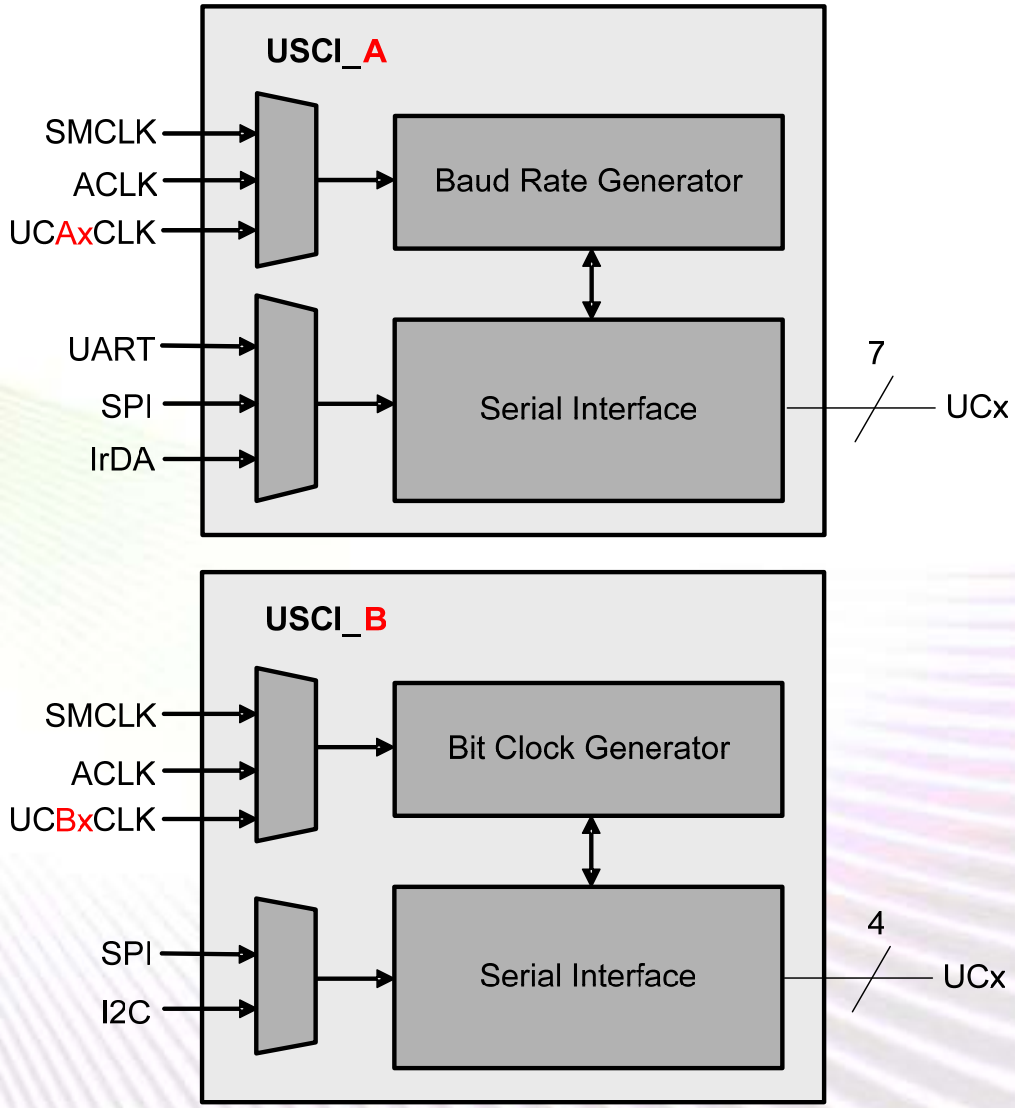
USI Clock Control



- **Multiplexed input from up to 8 int/ext sources**
- **Configurable divider**
- **Auto-stop on interrupt: USIIFG**
- **Selectable phase and polarity**
- **Software clock: USISWCLK clock input bit**

Universal Serial Communication I/F

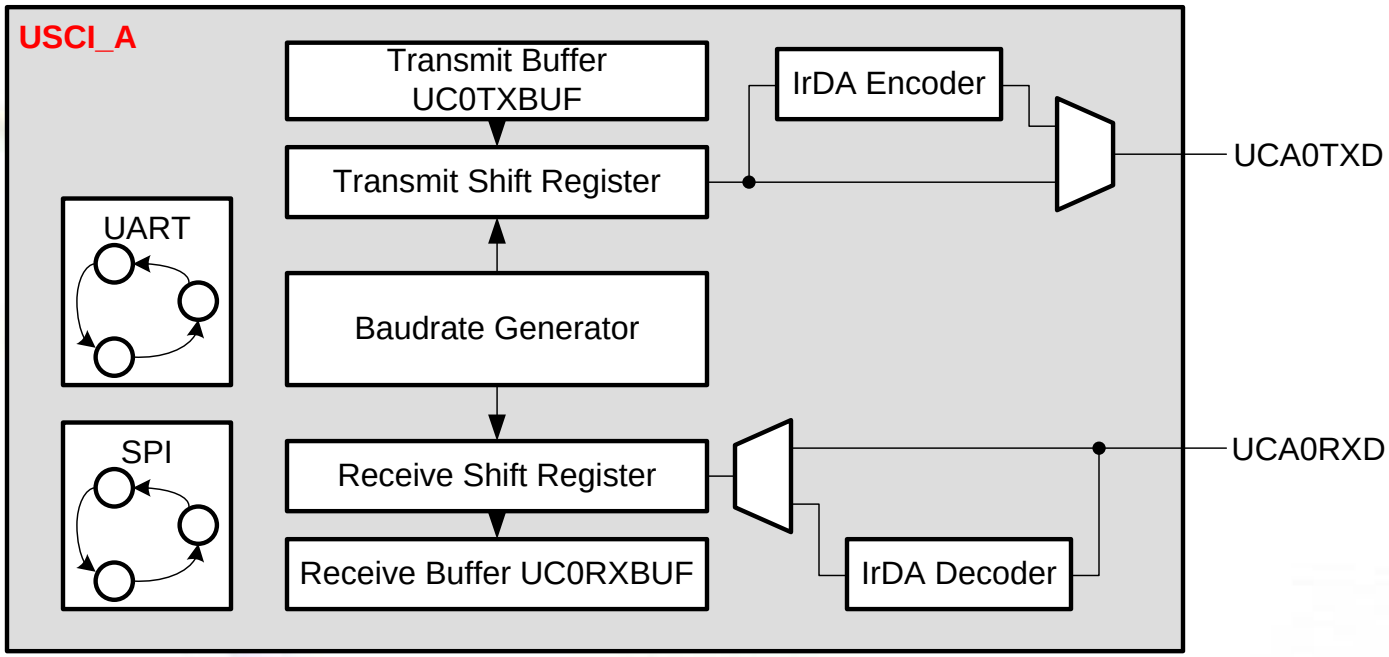
- **Ultra-low power**
  - LPMx operation
- **2 individual blocks**
- **Double buffered TX/RX**
- **RX glitch suppression**
- **Baud rate generator**
  - Flexible clock source
  - Automatic detection
  - Generation
- **DMA enabled**
- **Interrupt driven**



USCI Enhanced Features

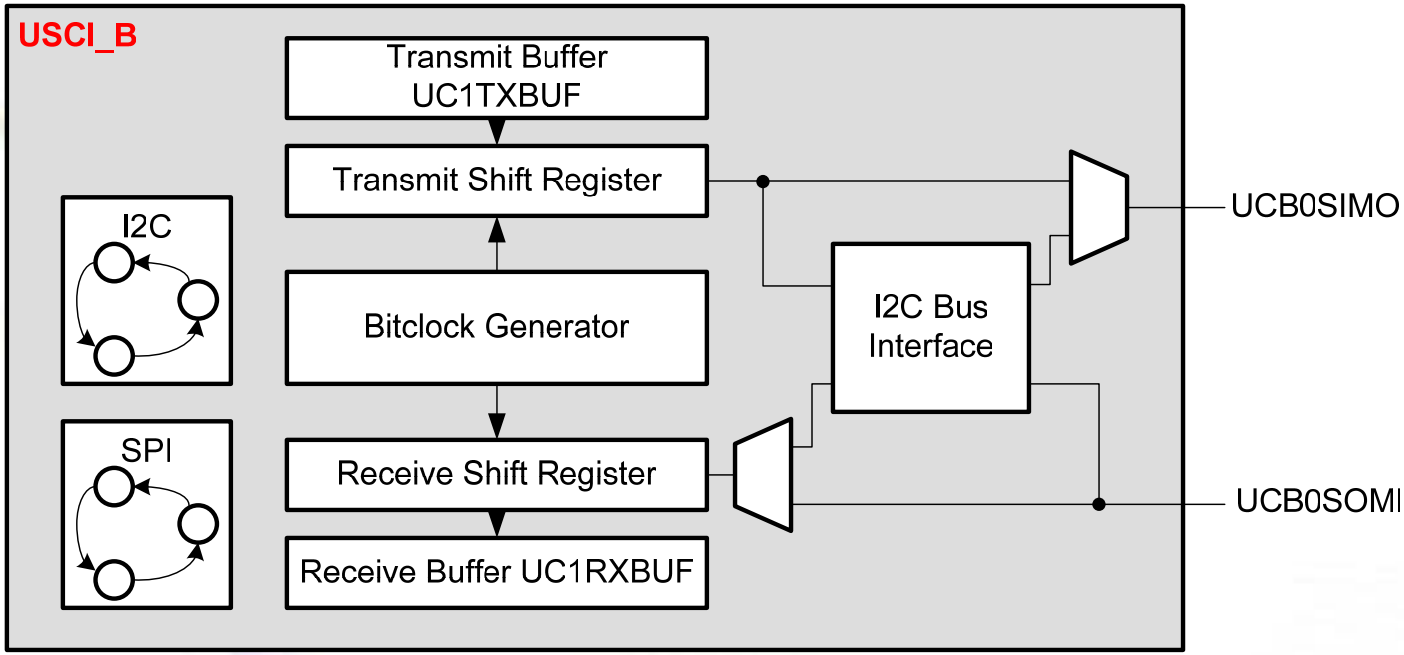
- **New standard MSP430 serial interface**
- **Auto clock start from any LPMx**
- **Two independent communication blocks**
- **Asynchronous communication modes**
  - UART standard and multiprocessor protocols
  - UART with automatic Baud rate detection (LIN support)
  - Two modulators support n/16 bit timing
  - IrDA bit shaping encoder and decoder
- **Synchronous communication modes**
  - SPI (Master & Slave modes, 3 & 4 wire)
  - I2C (Master & Slave modes)

USCI_A



- **UART with IrDA/LIN support or SPI**
- **Double buffered TX/RX**
- **Baud-rate generator with auto-baud rate detect**

USCI_B

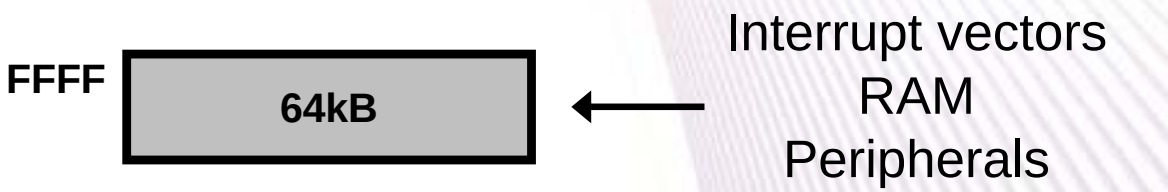


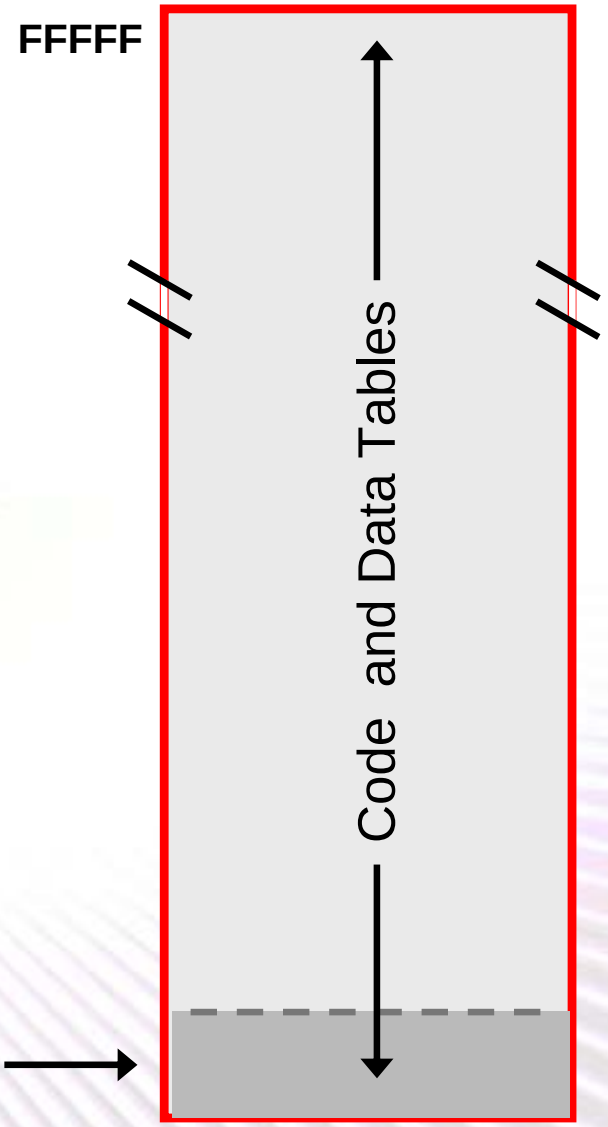
- **I2C master/slave up to 400kHz or SPI**
- **Bit clock generator**
- **Double buffered TX/RX**

New MSP430X CPU

- **Architecture upgrade**
- **100% code compatible**
- **1MB unified memory map**
- **Extended addressing modes**
  - Page-free 20-bit reach
  - Improved code density
  - Faster execution

MSP430F241x/261x



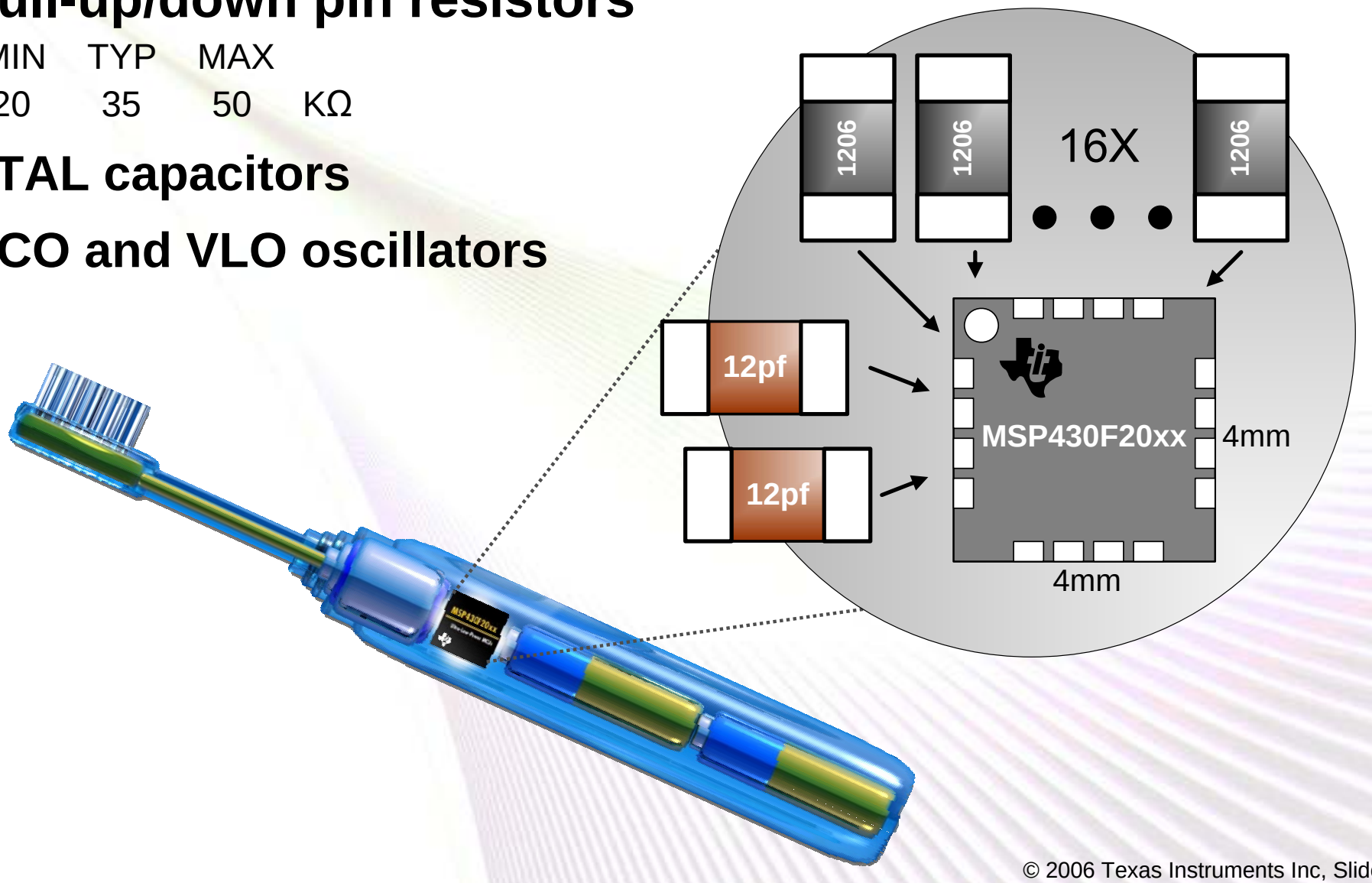


F2xx: Every Little Bit Counts

- **Pull-up/down pin resistors**

MIN	TYP	MAX	
20	35	50	KΩ

- **XTAL capacitors**
- **DCO and VLO oscillators**



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New F2xx Multi-Purpose Devices

Device	Pins	Flash/RAM	Features	Samples
F20x1	14	2KB / 128B	TA2, Comp_A	Now
F20x2	14	2KB / 128B	TA2, USI, AC10	Now
F20x3	14	2KB / 128B	TA2, USI, SD16	Now
F21x1	20	8KB / 256B	TA3, Comp_A	Now
F22x2*	38/40	32KB / 1KB	TA3, TB3, USCI, ADC10	Now
F22x4*	38/40	32KB / 1KB	TA3, TB3, USCI, ADC10, (2)OPA	Now
F23x0*	40	32KB / 2KB	TA3, TB3, USCI, Comp_A, MPY	1Q07
F23x*	64	16KB/512B	TA3, TB3, USCI, ADC12	2Q07
F24x*	64	60KB/2KB	TA3, TB7, (2)USCI, ADC12	2Q07
F241x*	64/80	120KB / 8KB	TA3, TB7, (2)USCI, ADC12,MPY	1Q07
F261x*	64/80	120KB / 8KB	TA3, TB7, (2)USCI,ADC12, MPY, (2)DAC12, (3)DMA	1Q07
All devices include enhanced watchdog timer (WDT+) and enhanced basic clock system (BCS+)				
* Planned Future device, in development				

Summary

- Pin-compatible drop-ins
- Lower Power
- Faster
- Many upgraded peripherals
- Many new devices

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