Combinational Logic

Task:

- Complete the truth table for a 2-bit comparator (Table 1) and write out the corresponding Boolean equations. Use these equations to describe the comparator in VHDL.
- Use "when .. else" VHDL statement to describe a 2-bit comparator.
- Use "with .. select" VHDL statement to describe a 2-bit comparator.

Table 1: Comparator Truth Table

in1	in2	eq_o	gr_o	ls_o
00	00	?	?	?
00	01	?	?	?
00	10	?	?	?
00	11	?	?	?
01	00	?	?	?
01	01	?	?	?
...	...	...	...	...
11	11	?	?	?

Perform functional simulation to verify correctness of the received VHDL descriptions. Implement and test the designs on FPGA development board. Compare implementation results of all three 2-bit comparators: in RTL Analysis and Synthesis schematics, Synthesis and Implementation reports, etc. How do they differ from each other? Prepare and submit a written report and project achives for the lab.

Creating Project Archive

For an easier project sharing or design relocation Vivado can create project ZIP archive. In the *File* dropdown menu select *Project -> Archive* option. In the *Archive Project* window (Figure 1) provide *Archive name* and *Archive location*. Uncheck *Include* options to exclude results of synthesis and implementation runs from the project archive. In this way only design source files will be included, thus archive size should be significantly reduced. Click *OK* to complete creation of the project archive.

Note, that simulation data would still be included in the project archive. It can also take a lot of space depending on the number of simulated signals and its duration. Remove *project_name.sim* folder from the project directory manually before creating the archive.

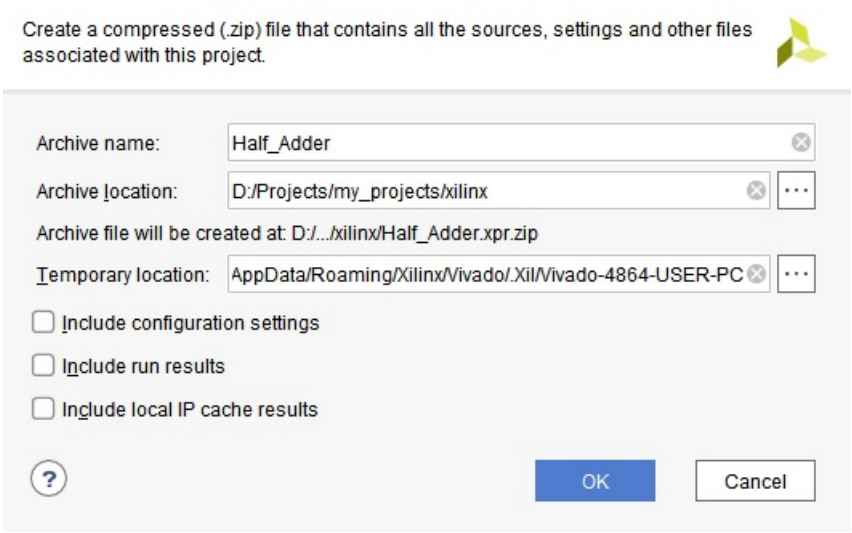

Figure 1: Archive Project Window