Logic Gates

Task:

Complete the truth table for schematic in Figure 1 (Table 1) and describe it in VHDL using dataflow style (i.e. with four concurrent assignments for each schematic block using VHDL logical operators). Use **std_logic_vector** type for describing inputs and outputs. Perform functional simulation to verify correctness of the received VHDL description. Use **assert** statements in the testbench. Implement and test the design on FPGA development board.

Table 1: Truth Table of Task Schematic

I(2)	I(1)	I(0)	T(1)	T(0)	O(1)	O(0)
0	0	0	?	?	?	?
0	0	1	?	?	?	?
0	1	0	?	?	?	?
0	1	1	?	?	?	?
1	0	0	?	?	?	?
1	0	1	?	?	?	?
1	1	0	?	?	?	?
1	1	1	?	?	?	?

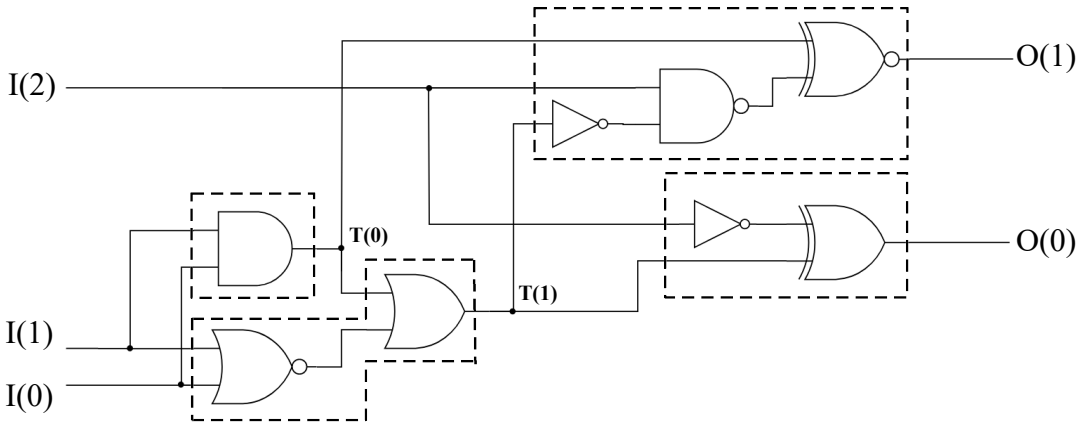

Figure 1: Task Schematic