# Research on Digital System Design and Test at Tallinn University of Technology

Raimund Ubar, Peeter Ellervee,Thomas Hollstein, Gert Jervan, Artur Jutman,
Margus Kruus, Jaan Raik

## 1. Introduction

We are entering the era of pervasive computing. PCs have been dethroned by technology to embed computers in almost everything. 98% of computers in the world are embedded. Massive amounts of electronics and software are controlling our everyday life. Pacemakers, cell phones, home appliances, energy generation and distribution, antilock brakes in cars – this is what we are depending on at every moment. We do not even notice this dependence, except when something is going wrong because of the computer crash. Embedded systems (ES) create both huge value for society, but also unprecedented risks because of possible errors and faults. We need dependability from the embedded computing world around us.

Silicon technology is continuously decreasing in size. According to the 2010 International Technology Roadmap for Semiconductors (ITRC), the industry should have the 22-nm technology by 2016. As critical dimensions reach the nanometer range, the devices will be subject to an increasing number of defects and intermittent faults during operation. Engineers are facing a paradox: they have to build reliable systems from unreliable components. From the development costs of systems, because of their complexity, up to 70% is going only for design verification and removing errors.

To cope with design verification and reliability problems, design for test and test synthesis methods are constantly evolving. New fault models have to be developed to handle new emerging defect mechanisms, and hierarchical approaches to synthesize automatically test programs is the way to deal with increasing complexity.

The research on digital hardware (HW) design and test in Estonia is concentrated mainly in the Department of Computer Engineering (DCE) at the Tallinn University of Technology (TUT), and is carried out in close cooperation with Estonian electronics industry especially with the companies like Ericsson, Elcoteq, National Semiconductor, Testonica Lab, and with R&D centres CEBE and ELIKO. In the following, an overview is given about the resent results in the field of design and test achieved in DCE and about the visions for future R&D in the field.

## 2. Overview of recent research

Our research has been concentrated on developing of new methods in design and test of digital HW regarding the topics in Fig.1.

### 2.1. Diagnostic modeling of systems

Traditionally, the theory of design and test of Digital Systems (DS) has been developed on the abstraction level of logic gate networks. To cope with the increasing complexity of systems, new high-level and hierarchical methods for diagnostic modeling of systems are emerging. On the other hand, shrinking geometries in nano-scale technologies produce new failure mechanisms which has forced to search for more advanced fault models. We have been looking for a uniform way of modeling systems

on different levels of abstraction. A solution has been found in developing a novel mixed-level graph-model in form of Decision Diagrams (DD).

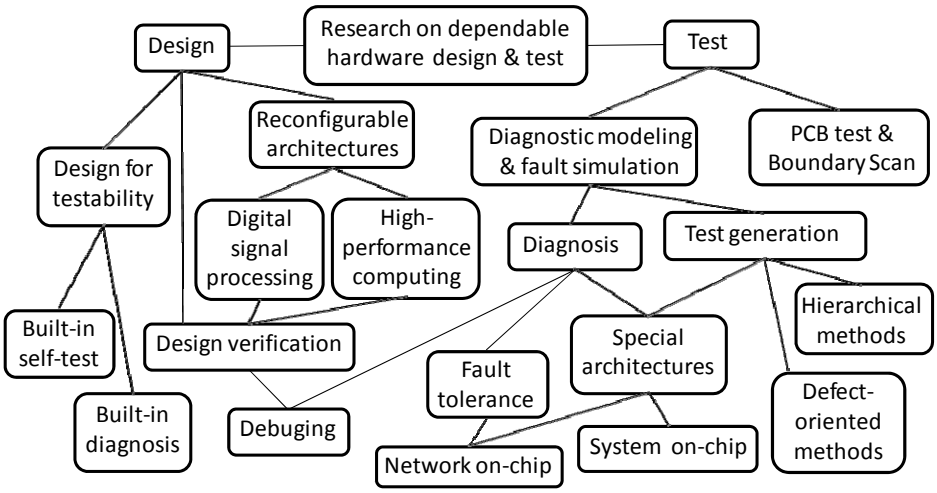


Fig.1. Research on dependable hardware design and test at TUT

Low-level modeling.

Binary Decision Diagrams (BDD) have become state-of-the-art data structure in VLSI CAD. BDDs were introduced in 1959 [1] for representing Boolean functions. For diagnostic modeling of digital circuits, a special type of circuit structure related BDDs were proposed at TUT in 1976 [2]. The first test generator in the world, based on BDDs, was built in a cooperation of TUT and Institute of Cybernetics in 1982.

After Bryant has shown in 1986 the simplicity of graph manipulations and proved the model canonicity [3], the BDDs started quickly to spread. However, traditional use of BDDs has been still functional, i.e the target has been to represent the functionality, and not the structure behind the functions as in Structurally Synthesised BDDs (SSBDD) developed in [2, 4, 5].

SSBDDs provide mapping between the graph and the related circuit, which allows to model different test relations and properties of circuits like signal paths, delays, faults, the properties of faults like masking, equivalence, dominance, redundancy, etc. These issues cannot be simulated explicitly with „classical“ BDDs. The motivation to introduce SSBDDs was to improve the efficiency of test methods by reducing the complexity of the model.

High-level modeling

To overcome the difficulties of high-level diagnostic reasoning of complex DS, we have introduced High-Level DDs [HLDD] as an extension of SSBDDs [4,6]. The model covers different levels of abstraction, and supports uniform fault analysis and diagnostic reasoning principles.

The most important impact of the HLDDs is the possibility of generalization of the logic level methods for using on higher levels by the same formalism. The class of variables was extended from Boolean to integer variables, whereas the class of Boolean functions was extended to data manipulation operations typically used in high-level descriptions of DS.

We have developed the canonical presentation of HLDDs in the form of characteristic polynomials [6].The synthesis of HLDDs can be carried out either by symbolic execution of procedures, or by iterative superposition of HLDDs, similarly to the synthesis of SSBDDs [7].

Both, SSBDDs and HLDDs have been the basis of a lot of research carried out in DCE to develop efficent methods and algorithms for automated fault diagnosis in digital systems.

Fault modeling and simulation

The DD-based fault modeling allowed us to improve the existing fault collapsing methods and to create a uniform fault formalism for different levels of abstraction [9]. It covers a broad class of faults like resistive shorts, opens and bridges [8]. To deal with the non-determinism of faults, the general Byzantine fault and *X*-fault models have been implemented with great success using SSBDDs for fault simulation purposes [9].

Fault simulation is the basic task in testing, and the fault simulators are used nearly in all CAD tools related to test. We have invented a parallel critical path tracing algorithm based on SSBDDs which allowed to speed-up simulation several times compared to the available commercial tools [7]. The main innovation was in the parallelization of analytical fault reasoning for many test patterns simultaneously. This idea was extended for general fault classes like conditional SAF [8] and X-faults [9].

## 2.2. Test and verification

A general formulation of the problem

Research in digital test is carried out in two main directions: test synthesis and fault diagnosis. Both problems can be regarded as reverse mathematical tasks. Consider a digital system in a very general form as a vector function $Y=F(X)$, where $Y$ and $X$ are the function and argument vector variables, respectively. A test experiment can be described as a diagnostic equation $F^*(X,dX) = dY$, where $F^*(X,dX)$ is a full differential of the system function, describing jointly the correct and faulty behaviours, where the vector differential $dX$ describes the possible faults, and $dY$ describes the result of test experiment in the form of possible deviations from the correct behaviour of the system. In the Boolean space the equation $F^*(X,dX) = dY$ takes the form of Boolean differential equation.

Without going into details, we can formulate now the two main test related tasks. The first is the direct task – to find $dX$ if $X$ and $dY$ are given, i.e. to locate the fault by the results of the given test experiment, and the second is the reverse task – to find $X$ if $dX$ and $dY$ are given, i.e. to generate test for the selected faulty behaviour.

Representing the reverse and direct tasks as the solutions of the same differential equation helps to have a uniform view on a lot of problems in testing: fault modeling, simulation and masking, test synthesis and analysis, fault diagnosis. For example, the fault simulation can be regarded as a special case of the direct task of fault location. The main problem is how to process the sequential behaviour of systems and cope with the complexity issues. In our research we have used DDs for solving the direct and reverse tasks of the diagnostic equation on different levels of abstraction.

Test generation

The test generation efficiency is sensitive to the complexity of the diagnostic model. On the other hand, the quality of tests is highly dependable on the accuracy of fault modeling. We have been targeting both, the efficiency by developing hierarchical approaches [10], and accuracy, by using conditional SAF [8].

The cornerstone of the defect-oriented test generation method [8] was the mapping of faults from one hierarchical level to another. Each library component is represented by a set of constraints calculated on the exact layout level. On the logic level, the physical defects are modeled by the constraints i.e. by conditional SAFs.

In [10] we developed a novel hierarchical approach to test generation for systems with mixed-level DDs. The method handles data and control parts in a uniform way. Experiments showed higher speed of test generation and higher fault coverage compared to the known academic tools. Commercial tools are

missing on the market. Based on the described method, a very efficient test generator DECIDER was implemented, and used for industrial designs at the Fraunhofer Institute Dresden in Germany.

New advanced methods for testing other classes of physical defects like shorts [8], crosstalks [11], and high-level functional faults [12] have been developed at DCE recently.

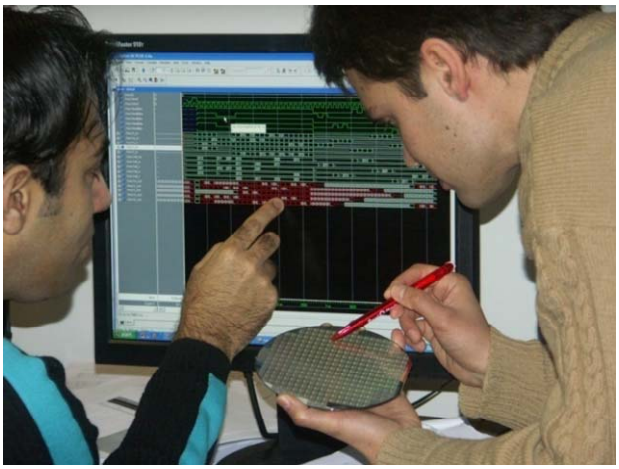

**Fig. 2.** Debuging errors in a digital design

Verification and design error diagnosis

SSBDDs and HLDDs have been used for improving the methods of design verification and error diagnosis at different system abstraction levels [13,14]. A novel approach for assertion coverage analysis targeted the quality assessment of verification stimuli and design error debug [13]. The approach considers HLDD-based design verification flow and relies on the extended HLDDs to support modeling of temporal properties.

Most research in design error and fault diagnosis has been done using specific fault and error models. But, the variety of design errors and hardware faults is practically infinite. A new method for debugging of errors, which does not use any error model was proposed in [14]. Based on a diagnostic reasoning of the circuit, a subcircuit suspected as erroneous is extracted. Opposite to known works, re-synthesis of the subcircuit need not be applied to the whole function of the erroneous internal signal in terms of primary inputs, it may stop at arbitrary nodes inside the circuit. As the result, the speed of repear will be significantly increased. The model free design error diagnosis method was extended also for using at higher levels of abstraction [7]. Since our method executes in polynomial time, the larger designs will be more efficiently handled by the proposed method than with the existing formal approaches.

Test methods

A new concept and a method for test and diagnosis was developed for NoC designs [15]. The method is based on functional fault models and it implements packet address driven test configurations. The approach is well scalable. The dedicated DfT techniques were proposed for application of test patterns from external boundaries of NoC. The experiments showed near-100% test coverage at the expense of less than 4% of extra switch area.

Electronic systems are usually based on SoC such as microcontrollers or signal processors that communicate with many peripheral devices on the system board and beyond. We pointed out particular challenges in testing of the printed circuit boards (PCB) and proposed a general modeling methodology for test automation for microprocessor SoC based system boards [16]. The method is a considerable

step forward in test automation, since today the test routines for PCBs are still programmed manually. We developed a new Boundary Scan (BS) based test access protocol for system-level testing of boards for manufacturing defects. The new technique dramatically extends the applicability of BS testing in complex on-board data buses and protocols. The side-effect of the technique is the possibility to increase the speed of in-system programming of flash memories where a speed-up of 50 times was achieved.

### 2.3. Design for testability

Hardware simulation

Meeting timing requirements is an important constraint imposed on highly integrated circuits (IC), and the verification of timing is one of the most critical tasks for CAD tools. The first time, a novel algorithm for multivalued simulation based on Boolean differential algebra for detecting hazards was implemented with SSBDDs in [5]. New algorithms were developed using SSBDDs, which allowed to speed-up timing simulation up to three times compared to gate level simulation [17].

Built-in self-test

New design paradigms like SoC and NoC have made external testing of systems increasingly difficult. The speed of SoC is constantly increasing and the technology used in external testers is always one step behind. Therefore, Built-In Self-Test (BIST) is emerging as a promising solution to the VLSI and SoC testing. We have developed different approaches to improve the efficiency and quality of BIST architectures. For the hybrid BIST which combines pseudorandom and deterministic test, a method and algorithms were developed for fast calculation of the cost of BIST to speed-up the solutions exploration [18].

A new approach to increase the speed of self diagnosis was developed, in which instead of the commonly used bisection of test patterns, the idea of bisectioning of faults was proposed [19]. To improve the diagnostic resolution, a novel approach of using multiple signature analyzers (SA) was developed. The key problem was to find an optimal interface between the circuit and SAs. An algorithm was created to find the optimal number of SAs for achieving the best diagnostic resolution.

Hardware based acceleration of fault simulation

Traditional SW-based simulators do not provide sufficient speed in case of complex systems. Especially time consuming is the BIST quality analysis in case of sequential circuits where test sequences are long and simulation speed is low. To achieve higher productivity in fault simulation, we developed a novel HW accelerator using reconfigurable logic on FPGA-s [20]. The proposed approach allowed speed-up of 40-500 times as compared to the SW-based fault simulation.

## 3. Potentials for future research

### 3.1. Research environment

A new modern embedded system research environment was recently established as the result of the project SARS, EU23626. Since 1995 our department is a member of EUROPRACTICE – a European Commission initiative which supports the cooperation between the selected universities and the electronic industry in Europe. As the result of this membership, CAD software from the most prominent EDA vendors, such as Cadence, Synopsys, Mentor Graphics, Xilinx has been installed in DCE. The environment includes as well the tools that have been developed in DCE as a side effect of research:

- TURBO -TESTER (TT) – for logic-level test [21,22];
- DECIDER – for hierarchical test generation [10];

- DOT – for defect oriented test [8];
- xTractor – CAD software for high-level synthesis;
- APRICOT – verification framework for high-level designs [13];
- DEFSIM – for research of the physical defects in integrated circuits [23];
- BIST Analyzer – a tool for research and analysis of the quality of BIST [24];
- Trainer 1149 – for investigating the basic concepts of the Boundary Scan standard [25];
- Java applets – for e-learning of logic and RT-level test [26].

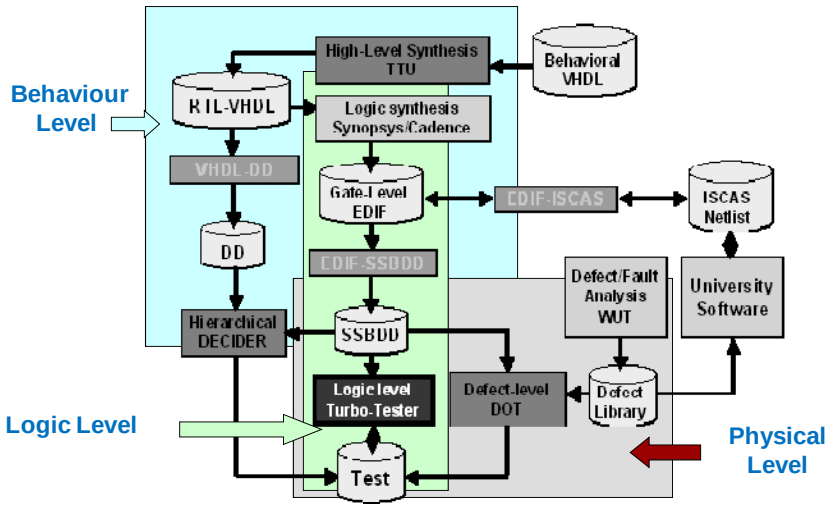


**Fig. 3.** CAD tool environment for research in HW design and test

TT has gained a large popularity all over the world, it has been licensed from more than 100 institutions in about 40 countries. The tools of TT allow to solve different test related tasks by alternative methods and algorithms in a wide scope of scenarios:

- test pattern generation by deterministic, random and genetic algorithms;
- test optimization and compaction;
- fault simulation by different algorithms;
- multi-valued simulation for analyzing dynamic behavior of circuits.

The tools of TT are based on SSBDDs, there are converters to link TT with commercial CAD systems. The tools support gate- and macro-level modeling. The latter helps to reduce the complexity of the model and to improve the performance. DECIDER uses two inputs – RT level descriptions in VHDL and low gate-level descriptions for components in EDIF. DOT is an extension of the TT for defect-oriented test. DEFSIM allows to carry out the low-level research of real physical defects to map them on the logic level. It is an HW/SW environment for experimental study of CMOS physical defects. APRICOT is an extension of DECIDER, to connect two communities – the hardware test community with the design verification counterpart. Trainer 1149 is a multi-functional SW system, which provides a simulation, demonstration, and CAD environment for learning, research, and development related to IEEE 1149.1 BS standard. BISTA and Java applets are a selection of tools that have been developed specially for teaching purposes, and are integrated into e-learning environment to support university hands-on training.

The originality of the environment is in its multi-functionality (important for research and training), low-cost and ease of use (Fig.3). The multi-functionality means that different abstraction level models can be easily synthesized (to analyze the impact of the complexity of the model to the efficiency of methods). Alternative methods for the same task are implemented to compare different algorithms, and the fault

models can be easily exchanged and updated to analyze the accuracy of testing. The multi-functionality allows to set up and modify easily different experimental scenarios for investigating new ideas and methods. In traditional commercial design tools these purely research and teaching oriented possibilities are missing.

### 3.2. Cooperation in the excellence centre CEBE

In 2008, a Centre of Integrated Electronic Systems and Biomedical Engineering (CEBE) has been established at TUT. It is one of the seven Estonian centres of research excellence, supported by EU structural funds, and it joins the research teams of DCE, Department of Electronics (DE), and Technomedicum (TM). The centre is carrying out interdisciplinary R&D in the fields of electronics, computer and biomedical engineering with applications in medicine, semiconductor and information technologies.

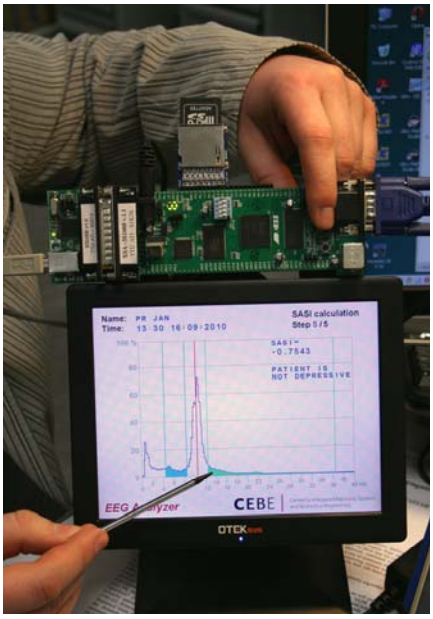


**Fig.4**. EEG analyzer detects depression

The research at DCE is greatly coordinated by the goals of CEBE, especially regarding applications. The partners of CEBE are also the founding members of the Competence Centre in Electronics, Info- and Communication Technologies ELIKO, which was established with the goal to develop innovative technologies and products, based on intelligent embedded systems, through strategic co-operation between the science and industry sectors.

The research cooperation in CEBE is organized in form of 7 internal projects targeting joint applications involving the partners' competences. DE provides knowhow in signal processing whereas TM involves experts from medical and bioengineering fields. A remarkable synergy has been achieved already in CEBE regarding joint design and test of biosignal processors for medical applications [27,28]. For example, based on the method invented in TM for detecting depressive disorders by measuring bioelectromagnetic signals of the brain [29], a mobile EEG analyzer is being now implemented in CEBE (Fig.4). Novel optical methods for estimating dialysis adequacy are being developed at TM [30]. Syrprising synergy has been shown in CEBE by implementing the ideas and models of diagnosis from the field of electronics developed in DCE for analysing the quality of dialysis in the medical field. CEBE is well cooperating with industry and hospitals.

### 3.3. International cooperation

The research team of DCE is characterized by active international cooperation. It has been involved in 14 EU-level projects within the COPERNICUS, COST, ESPRIT, FP5, FP6 and FP7 framework. Currently, two FP7 projects DIAMOND and CREDES are running, in both of them DCE is the coordinator.

DIAMOND (Diagnosis, Error Modelling and Correction for Reliable Systems Design) aims at improving the productivity of electronic system design in Europe by providing a systematic methodology and an integrated environment for the diagnosis and correction of errors. The consortium includes top-level research groups from universities of Tallinn, Linköping, Bremen, Graz, and the industry partners IBM, a leading microprocessor manufacturer, and Ericsson, a leader in the telecom field. Supported by CAD vendors TransEDA Systems and Testonica Lab, the team covers a full spectrum of the manufacturing chain from the tool development to the systems design and technology.

CREDES aims at creating a Centre of Research Excellence in Dependable Embedded Systems, based on the research potential of DCE, Dept. of Computer Science (DCS), and infrastructure of the Laboratory ASSA at TUT. The ambition is to become one of the Europe's leading institutions responsible for R&D in the areas of design, verification, test and diagnosis of ES. The Centre will be created by developing TUT's scientific expertise and capacities in collaboration with research groups at Universities of Verona and York, TU Darmstadt, and TU Brandenburg in Cottbus.

Cooperation with Testonica Lab and Göpel Electronic GmbH (Germany) has already resulted in two products „Microprocessor models for testing" and „Embedded instrumentation IPs for testing of electronic boards and chips" wich are marketed worldwide.

## 4. Future research directions

Our future research will target new breakthroughs in test, verification and dependability of embedded systems by developing new methods and CAD tools with design applications in health care. The research topics we are targeting belong to the forefront of scientific research and correspond to the priority research areas of roadmaps like ARTEMIS [31,32], ITRS [33], and HiPEAC [34].

### 4.1. Research perspectives for dependable embedded system design

Historical view on the vertical disintegration in IC Industry

Electronics industry has gone through major changes. Fig.5 depicts the developments in vertical disintegration of the semiconductor and electronic equipment design industry with predictions until 2020. In the beginning, microchips were completely designed and manufactured by integrated electronics companies. Equipment manufacturers were assembling chips to systems, and equipping them with the firmware and SW based on own developments. With increasing system complexity, the process of disintegration began on the ES market: semiconductor companies were offering their technologies to design companies by providing design libraries. Fabless semiconductor companies are offering own silicon products like FPGA. Currently, on the HW and SW side, many companies offer intellectual property (IP) components, which are used by system designers and system integrators to develop products efficiently in short development cycles. Such a disintegration will continue and in 2020 we expect the situation, that fabless companies will provide large scale reconfigurable platforms, consisting of fixed and reprogrammable HW as well as embedded processors (SW platforms). The platforms will enable opportunities for other companies to develop different applications.

The described development implies several economical and technical consequences:

- increasing system complexity requires new methods for integrated HW/SW design, which especially would address system reliability and dependability;

- system test strategies are required on all levels of design and integration, and powerful debugging strategies are crucial.

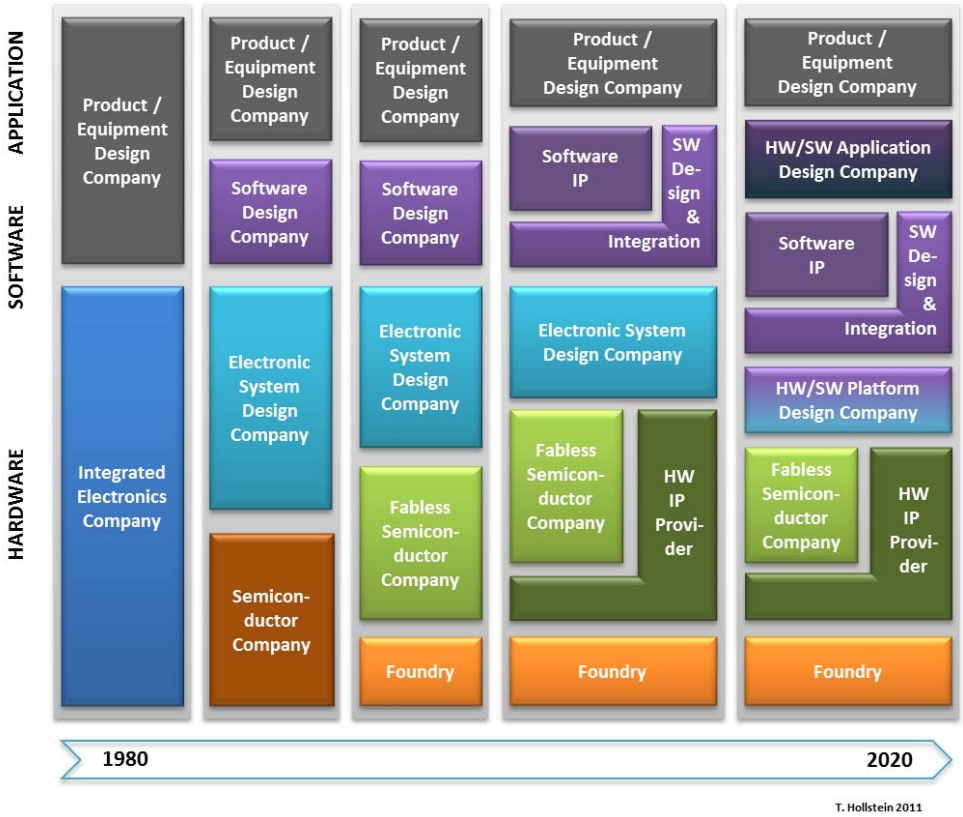


**Fig 5.** Vertical disintegration in semiconductor and electronics equipment industry

Consequences for industrial development and education

The vertical disintegration in the IC and IT industry generates a huge market for SMEs (especially important for small countries like Estonia), to offer own solutions in different stages of the IT product value chain. Fabless concepts allow successful business ideas for companies to offer HW IP components. Complete HW/SW platforms can be offered as fabless designs for customers targeting solutions in application areas. Highly sophisticated products can be developed based on available reconfigurable HW/SW platforms in cooperation with other companies.

In order to fulfill the requirements of future markets, the strategic education in universities and other educational institutions needs an early orientation towards the expected needs with respect to technical and professional skills. A key issue is, that while in the early stages of disintegration specific detailed know-how (HW or SW) was sufficient, future product development needs an increasing amount of system engineering. Highly skilled system designers who understand the components and methods coherences and who are capable to come up with system design decisions which match the constraints and requirements after the implementation and integration of all components, are needed.

Consequences for research in dependable embedded system design

The increased complexity of systems generates a demand for sustainable integrated HW/SW design methods with a strong emphasis on test, verification and dependability. Nano-scaled technologies with increased physical parameter variations have to be encountered with dependable circuit design methods in order to guarantee a sufficient yield and reliability of systems. Dependability concepts

cannot be limited to IC design, but have to be deployed on different levels of abstraction. Large-scaled future embedded platforms will comprise a large number of processor cores, specific HW components and reconfigurable HW. These numerous system components will communicate via flexible and scalable on-chip communication architectures such as NoC.

In our future research on dependable ES, we will focus on the dependability of HW components and adaptive NoC architectures, which allow to bypass faulty communication links and components, and novel application mapping methods on NoC-based multiprocessor platforms, considering reliability aspects.

### 4.2. Design research on dependable Networks-on-Chips

In the NoC-based systems the communication is achieved by routing packets through the network infrastructure, rather than routing global wires. However, communication parameters (inter-task communication volume, link latency and bandwidth, buffer size) might have major impact to the performance of applications implemented on NoCs. To guarantee predictable behaviour and to satisfy performance constraints of real-time systems, careful selection of application partitioning, mapping and synthesis algorithms is required. In the present, no methods or tools for solving these tasks for NoC-based real-time embedded systems exist.

Our approach will operate on a resource minimized NoC without virtual channels which are extremely area consuming. We assume to have NoC architecture with best-effort service without packet interleaving. A new concept for communication synthesis will be developed, which would not be run off-chip as a CAD tool on a workstation, but on-chip and being activated whenever the multi-core system is re-configured or new applications are added dynamically. The emphasis is on simple and efficient modelling and communication synthesis for dynamically reconfigurable systems, and the main idea is to calculate exact communication deadlines that describe how the communication synthesis can guide the scheduling process such that network conflicts can be avoided.

As technologies advance, a high degree of sensitivity to defects begins to impact overall yield and quality. The ITRS [33] states that relaxing the requirement of 100% correctness for devices and interconnects may dramatically reduce costs of manufacturing, verification, and test. Such a paradigm shift is likely forced by technology scaling that leads to more transient and permanent failures of signals, logic values, devices, and interconnects. It means that even in consumer electronics, for example, where the reliability has not been a major concern so far, the design process has to be changed. Otherwise, there will be a high loss in terms of faulty devices due to problems stemming from the nanometre manufacturing processes.

Due to the future design complexities and technology scaling it is infeasible to concentrate only to low level reliability analysis and improvement in system design. We have to target application level reliability analysis and improvement, i.e. we have to assume that the manufactured devices might contain faults and the application, running on the system, must be aware that the underlying hardware is not perfect. Moreover, design methods for dependable systems will have to cope with not only “failed” devices right after the production, but also with further failures in the field.

Hence, our future research will consider the topics of BIST, built-in self repair and recovery mechanisms that work in the field of application. In present, there is no complete system-level design flow taking into account the NoC modelling and system-wide dependability issues and therefore our main research effort will focus on various modelling and optimization methods that can be used for developing dependable, timing sensitive multi-core systems.

### 4.3. Application oriented design using reconfigurable logic

FPGA technologies have become a great potential to assist a general-purpose processors in performance-critical tasks which is often the case in ES. There are few reasons to use FPGA-s instead of general purpose processors or graphical processors. The first one is the flexibility of the reconfigurable fabric allowing implementing heterogeneous parallel computing units inside the same chip. Another reason, which is getting more and more important nowadays, is the energy efficiency – FPGA-s consume less power per operation than processors.

At DCE under coordination of CEBE, reconfigurable devices are planned to be used to accelerate calculations in different bio-medical measurement devices.

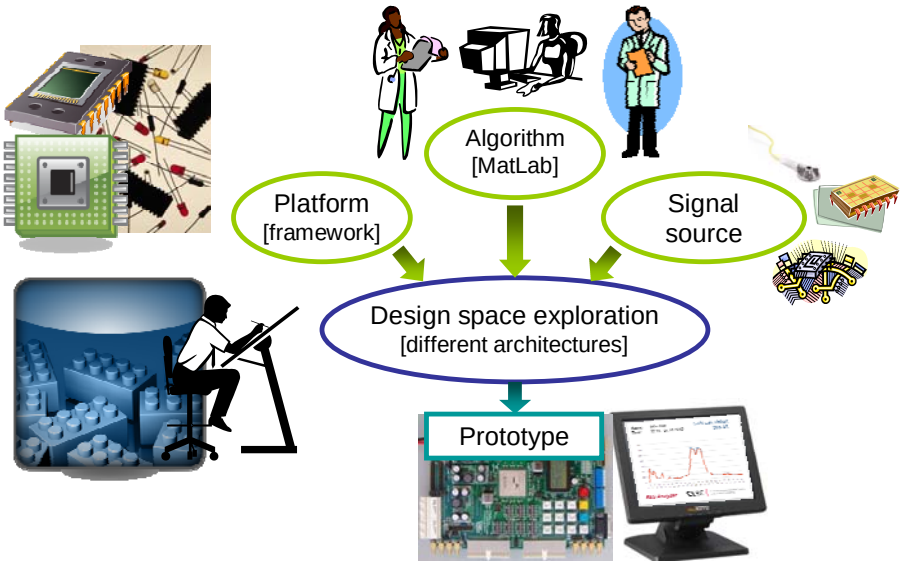


Fig. 6. Design platform for modular signal processing and reconfigurable logic based high-performance computing devices

Measurement of electrical bioimpedance enables to characterize a state of tissues/organs, to get diagnostic images, to find hemodynamical parameters, etc. The main problem with bio-impedance measurements is the fact that the useful information is hidden under the background noise generated by the normal body activity. An example would be respiration generated noise when measuring heart activities. The impedance of tissues and organs is measured between the electrodes having different locations. The response voltage is digitized into a uniformly sampled sequence of data that is processed in a Digital Signal Processor (DSP). Synchronous sampling can be extended to the multi-frequency measurement with the help of time-multiplexed sampling. A problem to be solved in sampling is to avoid aliasing effects. Promising results have been achieved already by implementing a preprocessing unit for eight-channel bioimpedance measurement device with 80 MHz sampling frequency using Xilinx Spartan3 FPGA.

Other design research plans are related to applications in the human brain research field. The analysis of human brain activity bio-signals requires complicated calculations and their interpretation remains to be a challenge for science. Everyday stress has made depression and other mental disorders to be more frequent. The method for detection of depressive disorder is based on analysis of the electroencephalographic (EEG) frequency spectrum and is capable of determining depressive disorders. A spectral asymmetry index (SASI), developed in CEBE [29] is used as a depression indicator, and can be calculated as a relative difference in power of two EEG special frequency bands selected higher and

lower of the EEG spectrum maximum. The main challenge will be to develop a portable device which would offer real-time analysis and acceleration of the calculation procedure.

Similar devices based on DSP modules and implemented as reconfigurable architectures can be easily adjusted on-the-fly for solving other tasks in health monitoring.

The results of the research described will be used in future work to define a modular signal processing platform (Fig.6) and its components for reconfigurable logic based high-performance computing devices. The platform will consist of communication network, sensors/actuators, and signal processing units. While the sensors and actuators can be seen as more-or-less standard devices, the other parts must be configurable to allow to make trade-offs depending on the design constraints. The constraints can be performance, energy consumption, data format, etc. Some applications may need point-to-point fast cross-bar networks while other applications can work with slower but cheaper bus-like networks. The same applies for the processing units where a good example is Fast Fourier Transform that can be implemented in very many configurations depending on the performance and window size requirements, for instance. The research will focus on analyzing the requirements of different signal processing applications to identify the needs for parameterization and developing parameterizable network and processing modules.

### 4.4. Future research challenges in system test and verification

The cost of designing nano-scale chips is rapidly increasing. Together with the growth of design complexity, the design methods as well as test and verification methods have to shift to higher abstraction levels. In particular, transaction-level modeling at Electronic System Level is gaining ground in modern design process.

There is a need for new verification methods that would operate on higher abstraction levels and provide readable and compact information for the design engineer. The feedback from existing verification solutions is far too detailed and contains too much data. This makes understanding the root causes of errors and debugging in complex systems an overwhelming task. Similarly, the test methods have to move to higher levels. At the same time there are challenges emerging from the lowest abstraction levels because of new effects in nanometer technologies like process variations, power consumption, or vulnerability to crosstalk effects. More emphasis should be put on functional, and at-speed test as they tend to cover more defects than the conventional methods. New failure mechanisms are essentially dynamic, not static, and delay faults are gaining importance. The power dissipation has become a serious issue and power-aware testing methods are becoming inevitable.

According to Rent's Rule the number of input/output terminals of chips grows as a square root with respect to the number of transistors. This implies that the test access is going to be more and more difficult. BIST is required to provide test access to modern systems and to test them at-speed.

Soft errors caused by radiation effects are becoming a severe issue in nanometer processes. This means that it will not be possible to create working miniaturized electronic circuits anymore without implementing fault tolerant techniques.

Finally, adoption of 3D stacking process in chip manufacturing causes a paradigm shift in test. Test access will be a problem. When you are doing a wafer test then you cannot really access the contacts without proper pads. It is not possible to probe the Through-Silicon Vias (TSVs) due to the small size and low fracture strength of micro-bump contacts. The community is forced to apply scan-path, BIST, test compression and other DfT solutions. Therefore, the re-use of DfT on different dies becomes essential. Serious problems remain with signal integrity and power integrity.

The considerations above will determine our future research in test, verification and fault diagnosis. To cope with the complexity of problems, we will use hierarchical approaches. To handle the problems of

diagnosis at different levels of abstraction, we will use the theory of multi-level decision diagrams which, however, needs extensions and further developments. Fault simulation is the basic tool in all test related tasks. We have achieved good results in logic level fault simulation, however, these results must be extended to support higher level verification and debugging to cope with the complexity.

### 4.5. Challenges in testing of complex electronic boards

The electronic industry is entering a new age, where static structural test technologies like Boundary Scan (BS) and In-Circuit Test are quickly losing their efficiency in terms of fault coverage, while no systematic alternatives to replace them currently exist. This brings up a lot of concerns in the industry and needs a due attention from academic researchers.

Various solutions exist for manufacturing defect testing on complex PCBs, but all of them have certain limitations (low fault coverage, low speed, expensive equipment). As a result, numerous production test types/test phases have to be used, which turns testing into a time-consuming and expensive process. As modern systems become “smarter” and more complex, traditional production tests are losing in quality and efficiency in terms of fault coverage. BS has shown good diagnostic capability, but is also essentially slow. We are aiming to extend BS applicability to high-speed testing, yet keeping the good diagnostic properties and low cost of equipment.

Despite of constantly improving test automation solutions, the new technological reality elevates the cost of testing. Due to usage of numerous production test types/test phases and a time-consuming testing process, new electronic products need a longer time to reach the market. The mentioned problems are getting even more critical taking into account the fact that system integration has taken the path of the emerging 3D chip technology.

Our future research will target the testability problems in emerging high-performance design architectures - 3D chips and advanced system boards. This will be the basis of future development of an automated and relatively low cost test solution that guarantees a good fault coverage and diagnostic resolution. Our goals are to develop embedded test instruments beyond the state-of-the-art targeting unsolved test challenges especially those applied to 3D architectures, and a new technology that would enable generating adaptable instrumentation cores.

## 5. Conclusions

The primary objective of our future research will be to develop methodologies for designing reliable applications out of non-reliable hardware. In the long term, the obtained solutions will be fundamental in the emerging paradigm of massively parallel computational devices.

The general impact of our research lays in the development of new efficient methods, algorithms and tools for design and test of dependable and mission-critical embedded systems with the goal to reduce time-to-market, cost and improve the quality of applications.

This research will be important for the development of Estonian economy and for the whole society. As a short-term importance, the outcomes can be used in electronics industry and improve its competitiveness in the international markets. The developing scientific excellence will help to strengthen the quality of university teaching for educating students with professional skills. As a long-term impact, new competitive spin-off SMEs are expected to appear in the Estonian electronics industry.

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