"Analog & Mixed-Signal Circuits Testing"

Sergey G. Mosin, Vladimir State University

The Contents:

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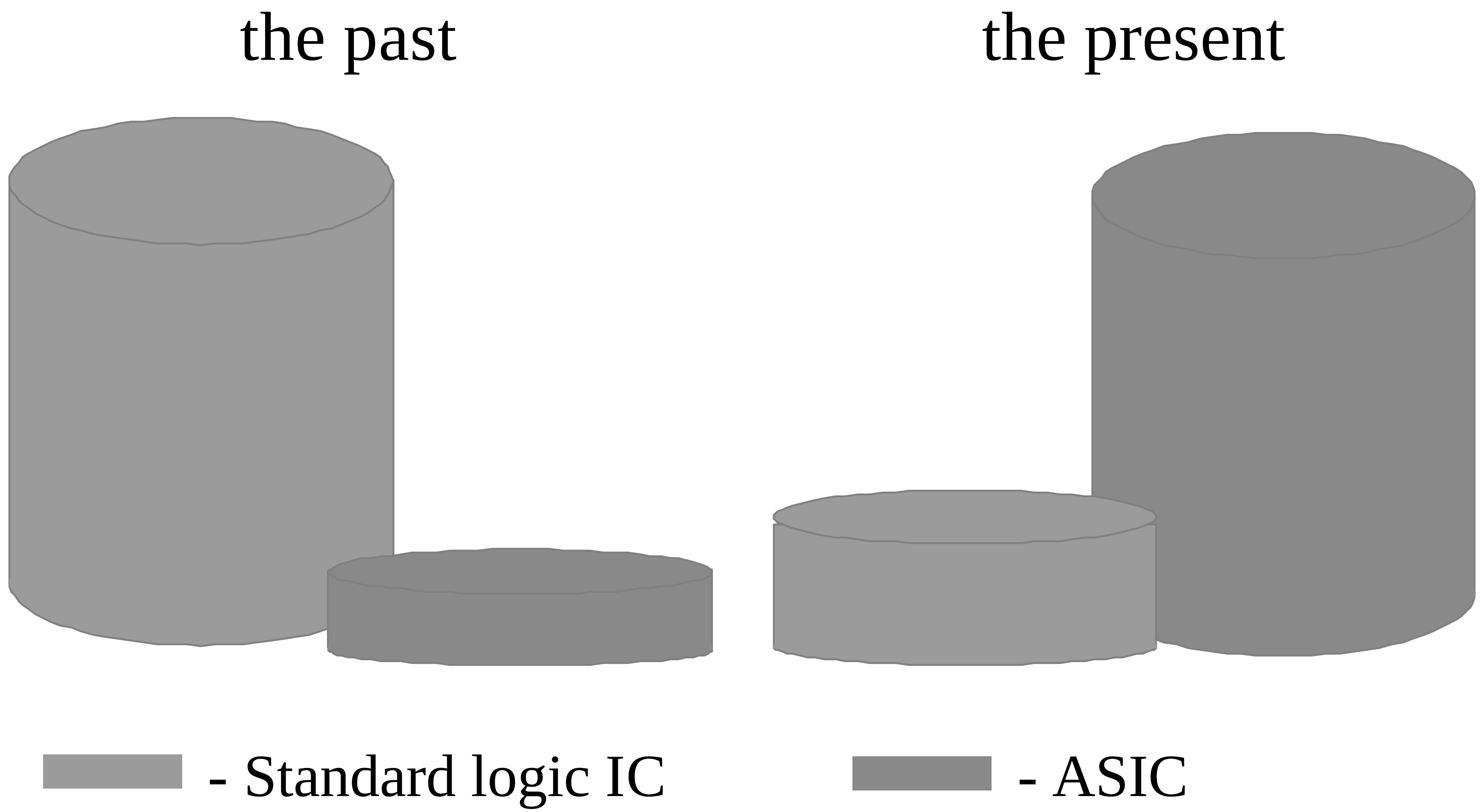
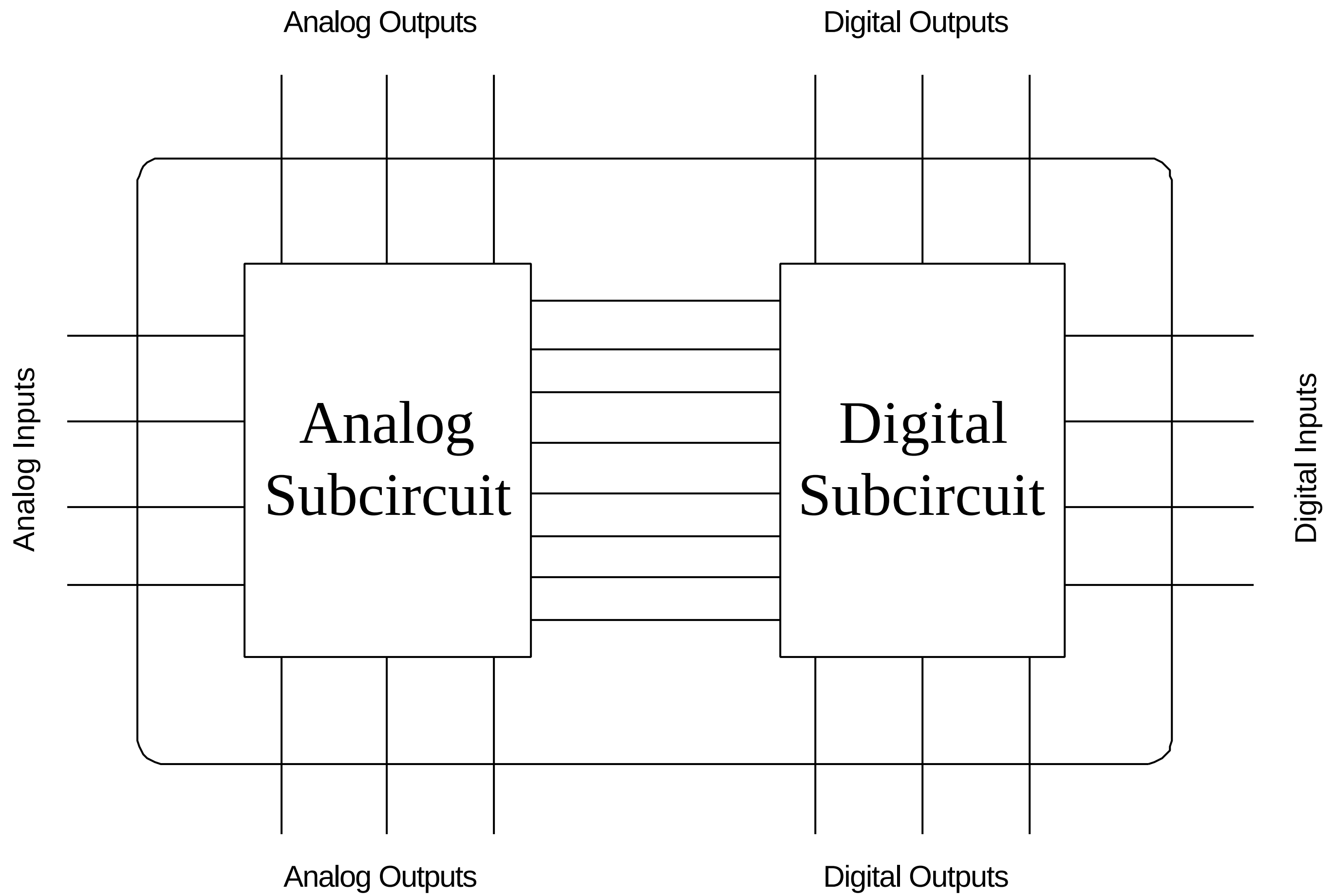
Introduction:

The features of IC manufacturing



Introduction:

Mixed-Signal Integrated Circuit



Introduction:

The applications of Digital Signal Processing

- Multimedia;
- Computer networks;
- Telecommunications;
- Consumer Electronics;
- Avionics;
- Biomedical Tools, etc.

Introduction:

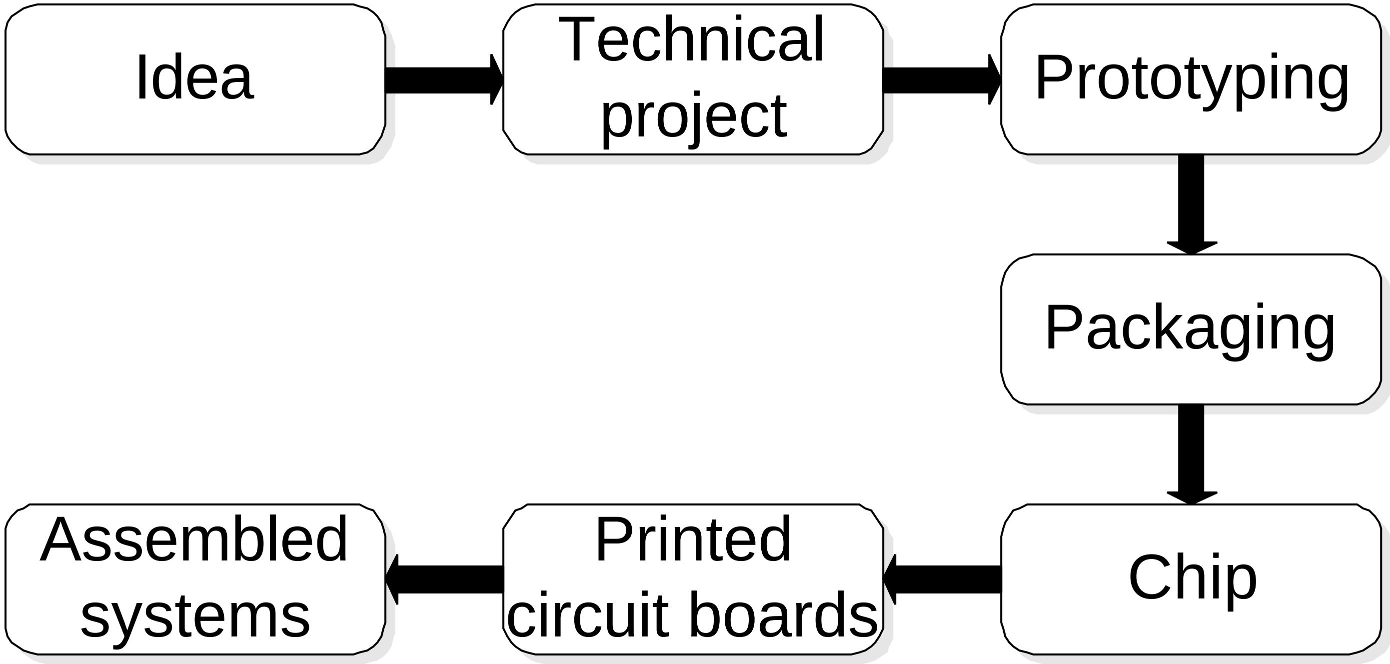
The advantages of Mixed-Signal IC usage

- Minimization of signals distortion;
- Miniaturization of complete devices;
- Reduction of complete devices' cost,

  etc.

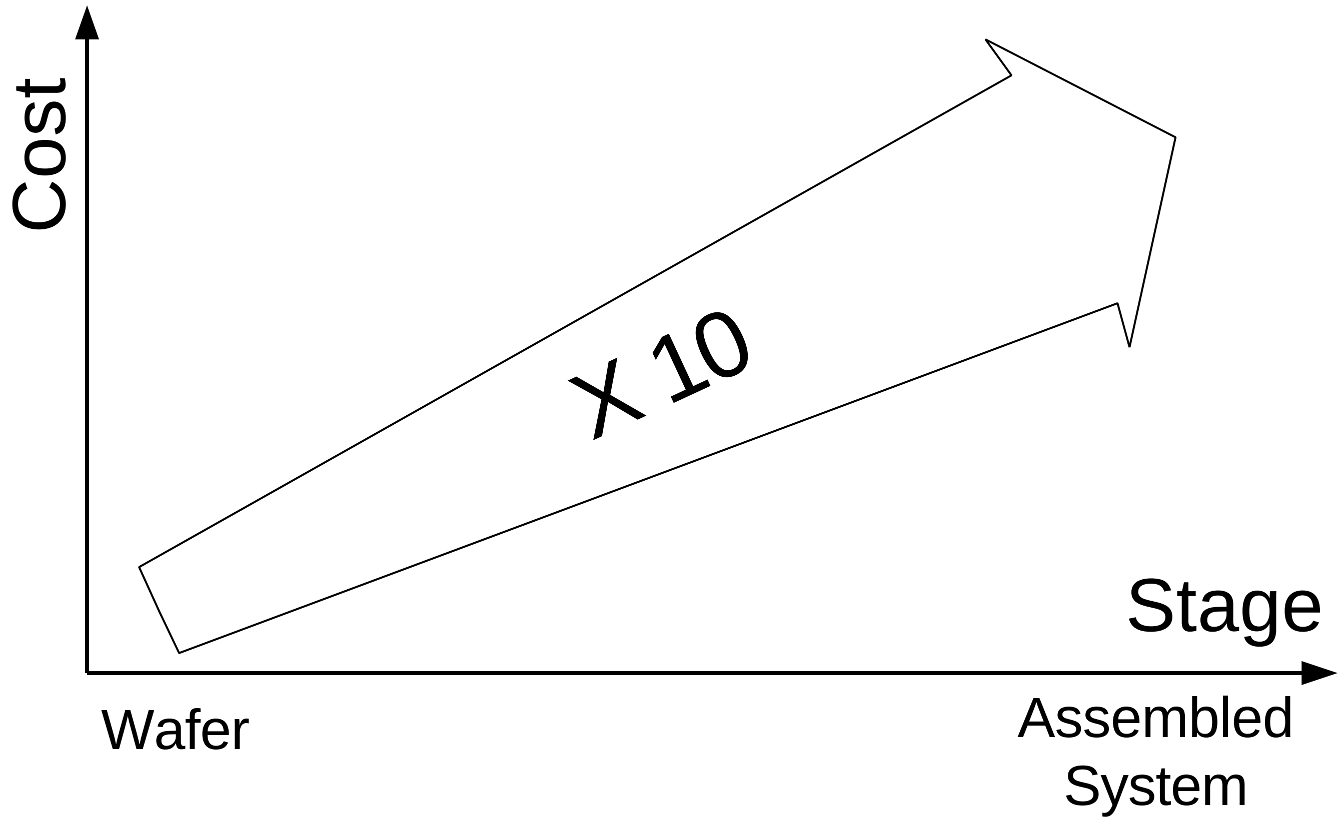
Introduction:

The production stages of electronic devices



Introduction:

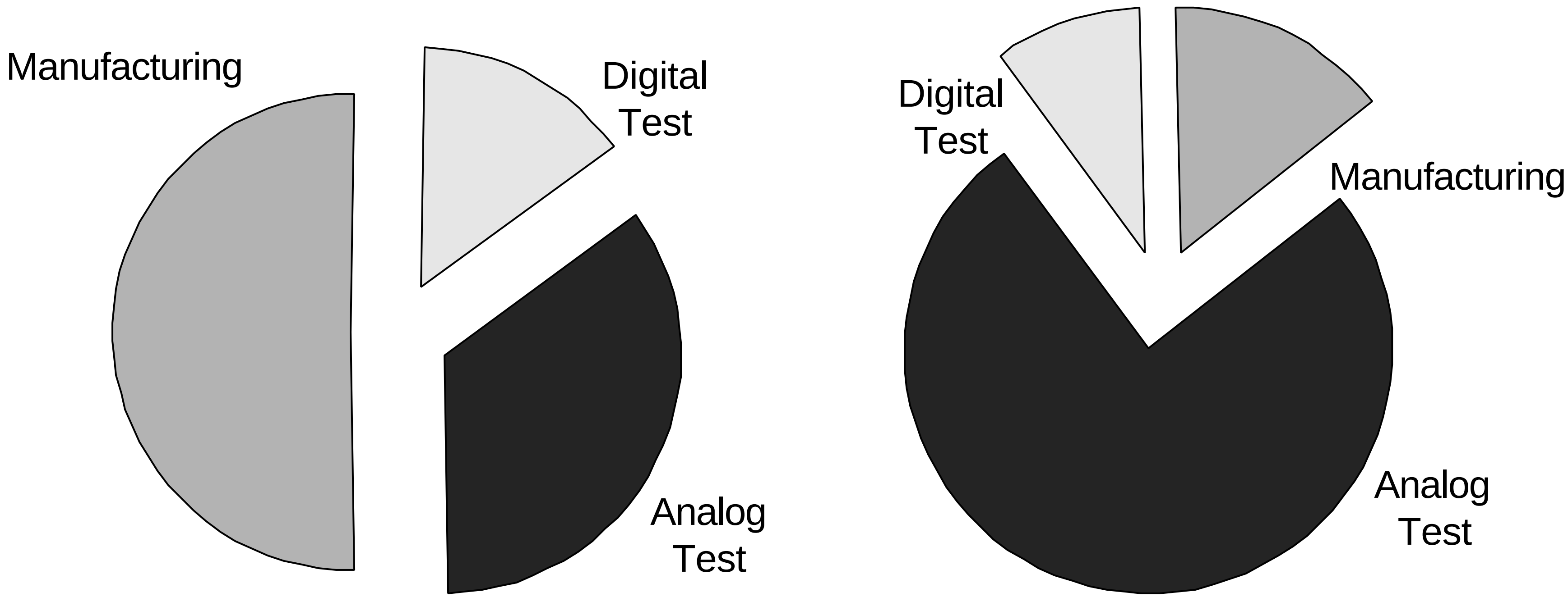
The rule of ten



Introduction:

Relative product cost for a mixed-signal IC

present day future



Introduction:

The complexity of IC testing

- The changes in the technological process;
- The growing scale of integration;
- The rise of functional complexity ;
- Absence of access to internal components and nodes of the circuit, etc.

Introduction:

The ways for reduction of a test cost

Design-For-Testability (DFT)

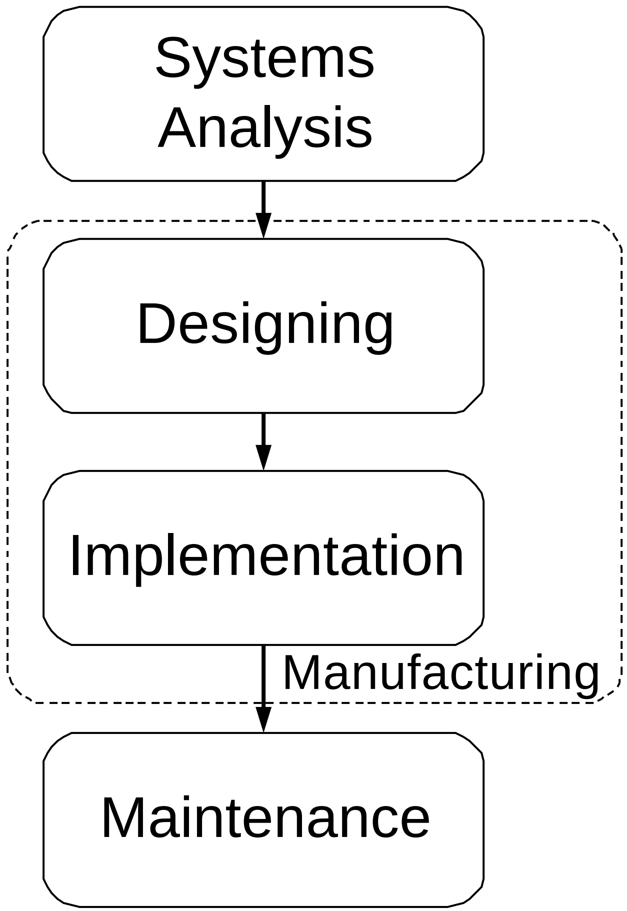
investigation of possibilities and preparation of the recommendations for electronic device testing during early stages of its designing

Automated Test Pattern Generation (ATPG)

automation of test development process and testing realization, development and improvement of modern computer-aided test generation systems

The place of testing in IC's life cycle:

Life cycle of IC



The place of testing in IC's life cycle:

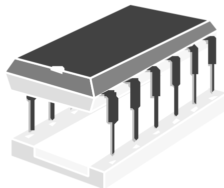
The kinds of testing

Verification

Test

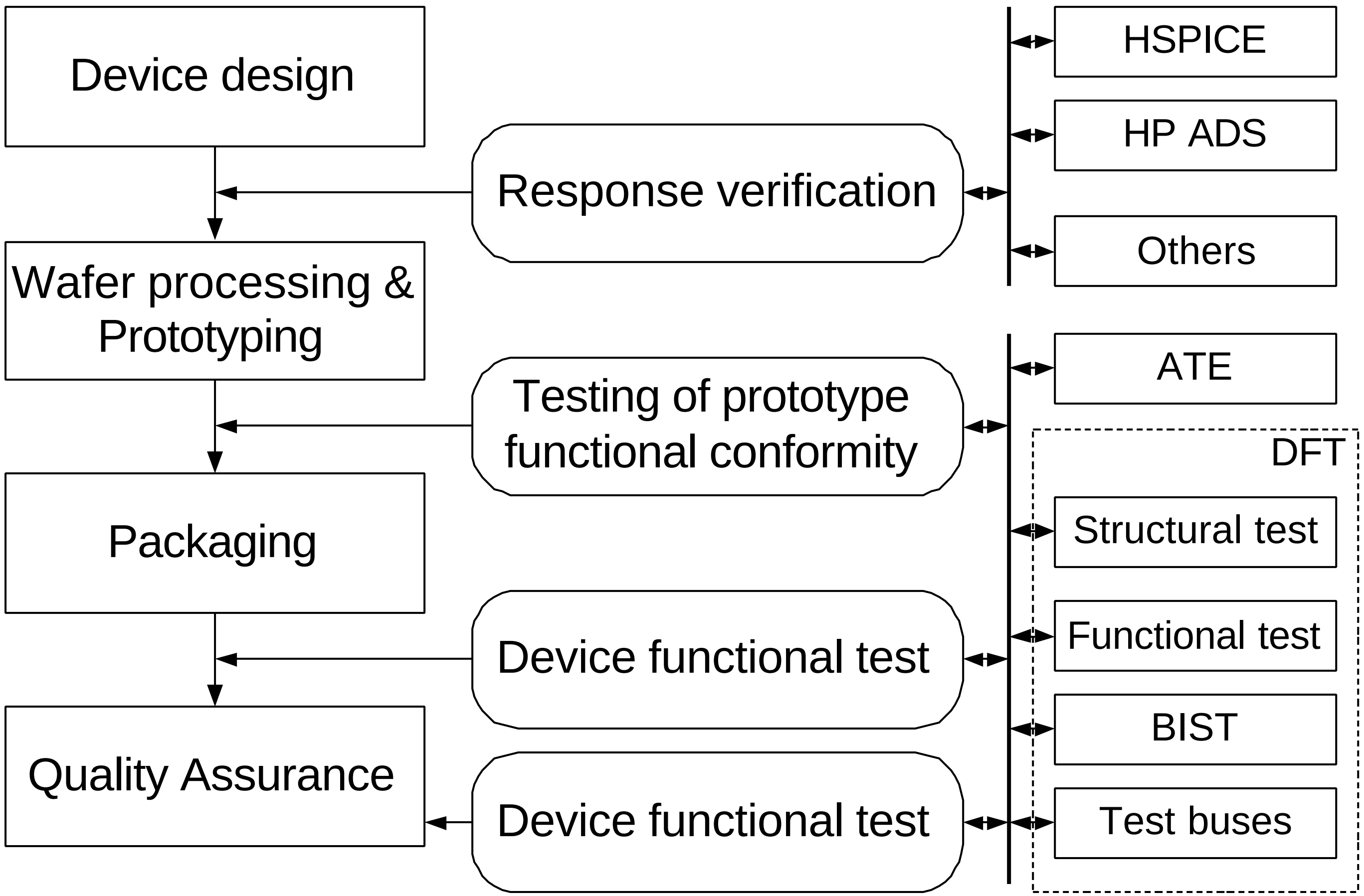
Diagnosis

Localization



The place of testing in IC's life cycle:

Testing of IC on different manufacturing steps



The place of testing in IC’s life cycle:

Device design verification

- Working mode of the device is simulated;
- The best and worst cases of its operation are studied;
- Making a decision about device functionality, quality of executed functions, and their correspondence to the initial requirements.

The place of testing in IC's life cycle:

Wafer processing and Prototyping

- The prototyping of the developed device in a chip is executed;
- The functional correspondences of parameters and characteristics for each die on a wafer are defined;
- The unsuitable devices are marked for culling on the future step.

The place of testing in IC's life cycle:

Packaging

- Cutting of a chip wafer on independent dies;
- Devices that successfully have passed testing on previous step are packaged;
- Testing of packaged device guarantees correspondence of functions, executed by the device, and also quality of internal wire bondings and operation of packaging in whole.

The place of testing in IC's life cycle:

Quality Assurance

- Setting and adjusting of the technological equipment for the mass production of ICs;
- The testing of the device on this step provides guaranteed quality of released production and inspects possible deviations of the technological manufacturing equipment from normal operation.

Classification of defects:

Fault in a common case is understood as such change of the element characteristic to its nominal value, which can cause violation or refusal in operation of a whole device.

From the point of view of trouble shooting the major parameter of a fault is the time of its existence:

$$T_{ex} = T_{det} + T_{loc} \quad ,$$

where

T_{ex} is a time of fault existence;

T_{det} is a time of fault detection;

T_{loc} is a time of fault source localization.

Classification of defects:

Different kinds of defects classification

- Based on temporal parameters;
- Based on frequency of defects appearance;
- Based on the number of defects presence in the device;
- Defects of the manufacturing process.

Classification of defects:

Based on temporal parameters

Fail or Breakdown

$$T_{ex}^{fail} \geq T_{det} + T_{loc}$$

Failure

$$T_{ex}^{failure} < T_{det} + T_{loc}$$

Classification of defects:

Based on frequency of defects appearance

<u>**Single**</u>

(not arise any more after restoring of the device serviceability)

<u>**Frequent**</u>

(arise with some periodicity)

Classification of defects:

Based on the number of defects presence in the device

<u>Single</u>

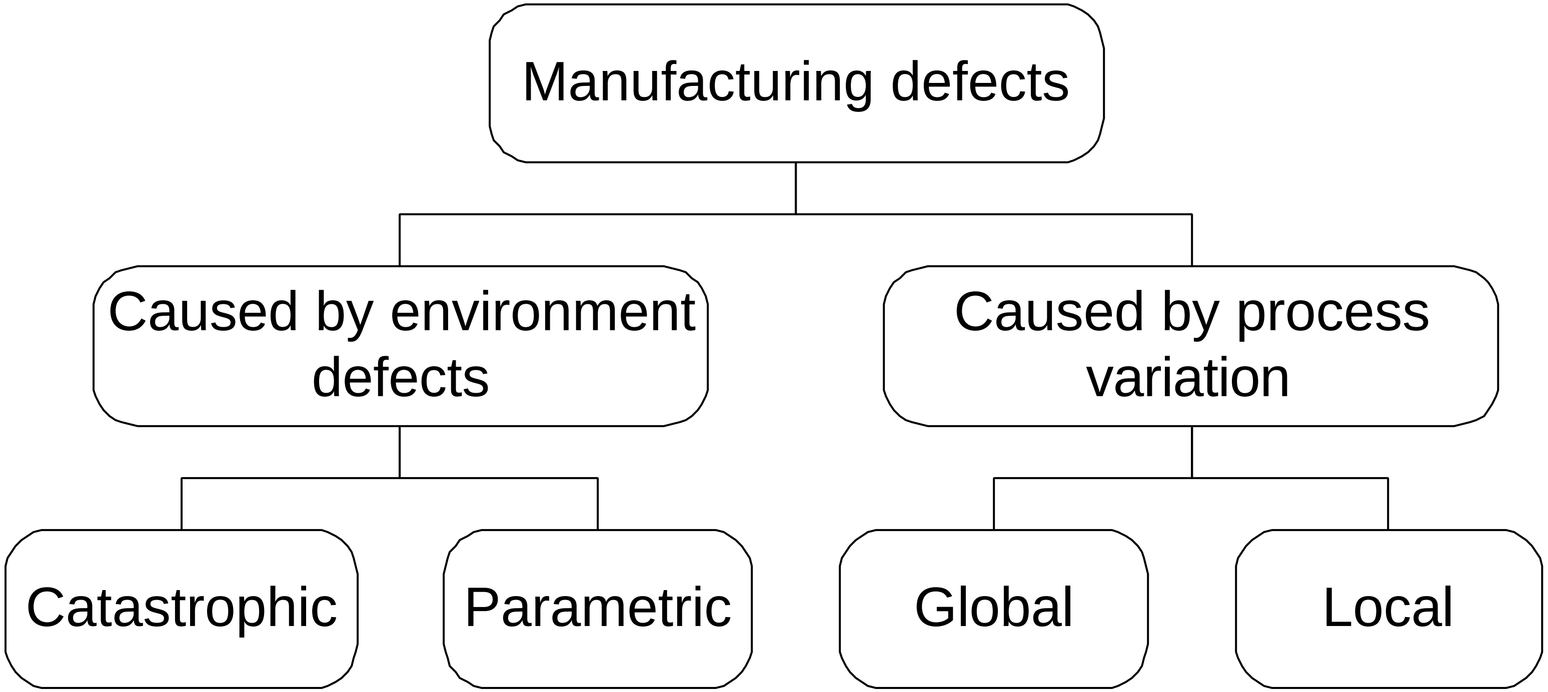
(defined by change of only one internal parameter)

<u>Multiple</u>

(defined by simultaneous change of several internal parameters)

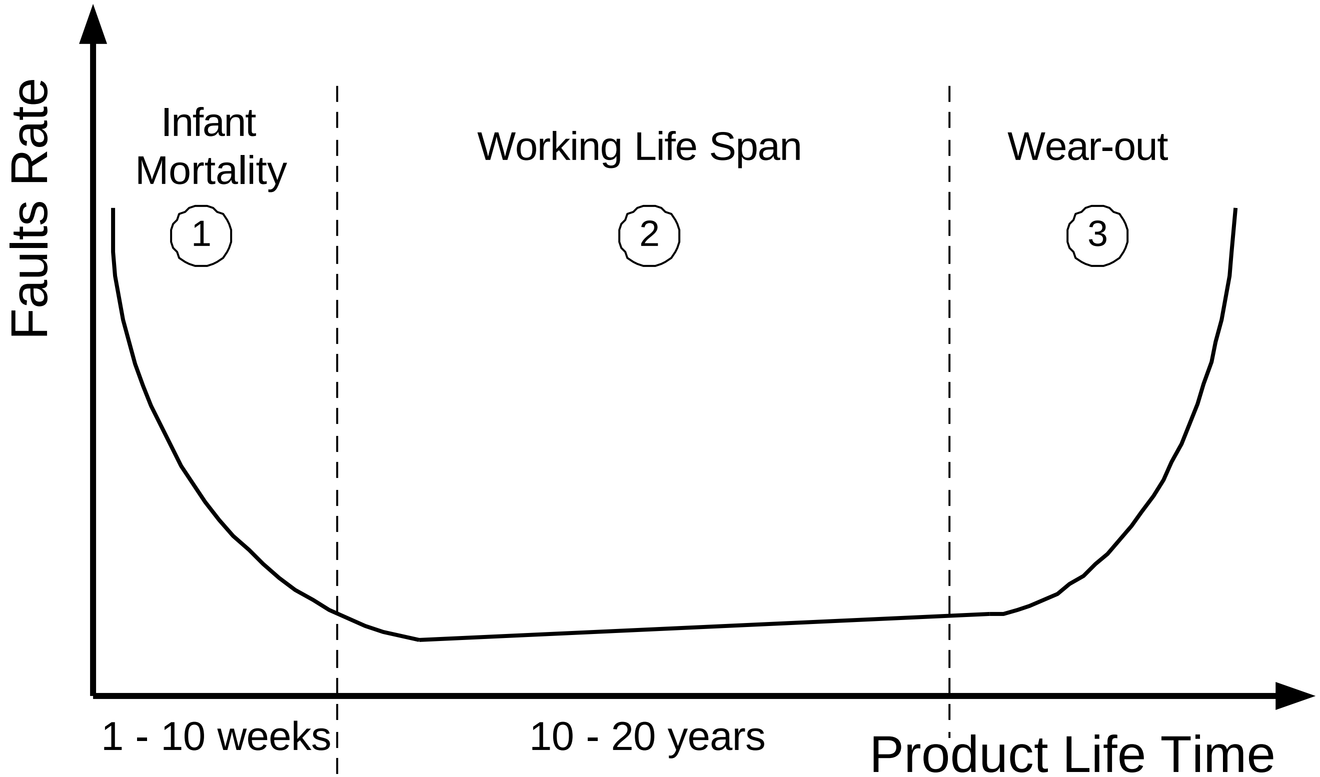
Classification of defects:

Defects of the manufacturing process



Classification of defects:

The intensity of fault appearance during life cycle of electronic devices



Classification of defects:

Qualitative measures of electronic devices

The ***reliability*** is an ability of the device or system to save the functionality during some period of time without occurrence of faults.

The ***wearing capacity*** is an ability of the device to resist to processes of aging and wear of the equipment.

Classification of defects:

The estimation of a reliability can be executed by statistical methods in the form of the durability test.

*If in a batch from **N** pieces during time **t** take place **n** fails, then the intensity* l *of fails can be estimated as*

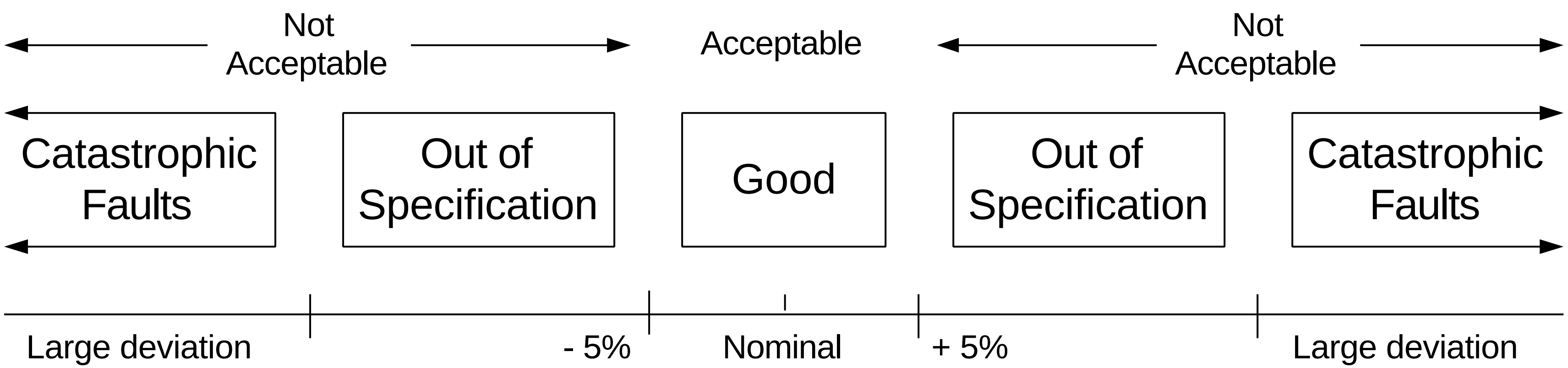
$$\lambda = n/(Nt)\ .$$

Knowing the value l, *the probability of non-failure operation of ICs during the given time of maintenance **t** can be estimated as*

$$P = e^{-\lambda t}\ .$$

The faults of the analog circuits:

Classification of analog circuit faults

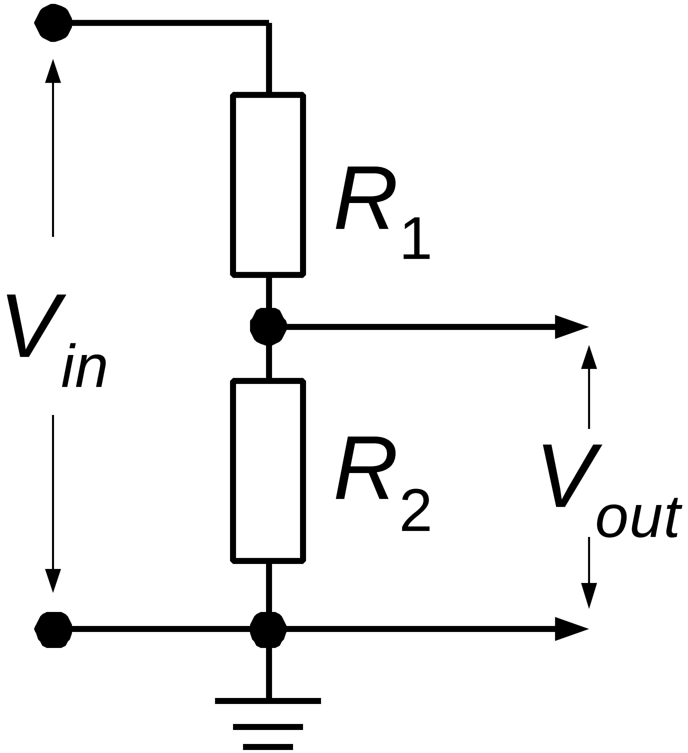


The faults of the analog circuits:

Example: the elementary circuit of potential divider

The relation between input and output voltages is defined as follows:

$$V_{out} = \frac{R_2}{R_1 + R_2} V_{in}$$



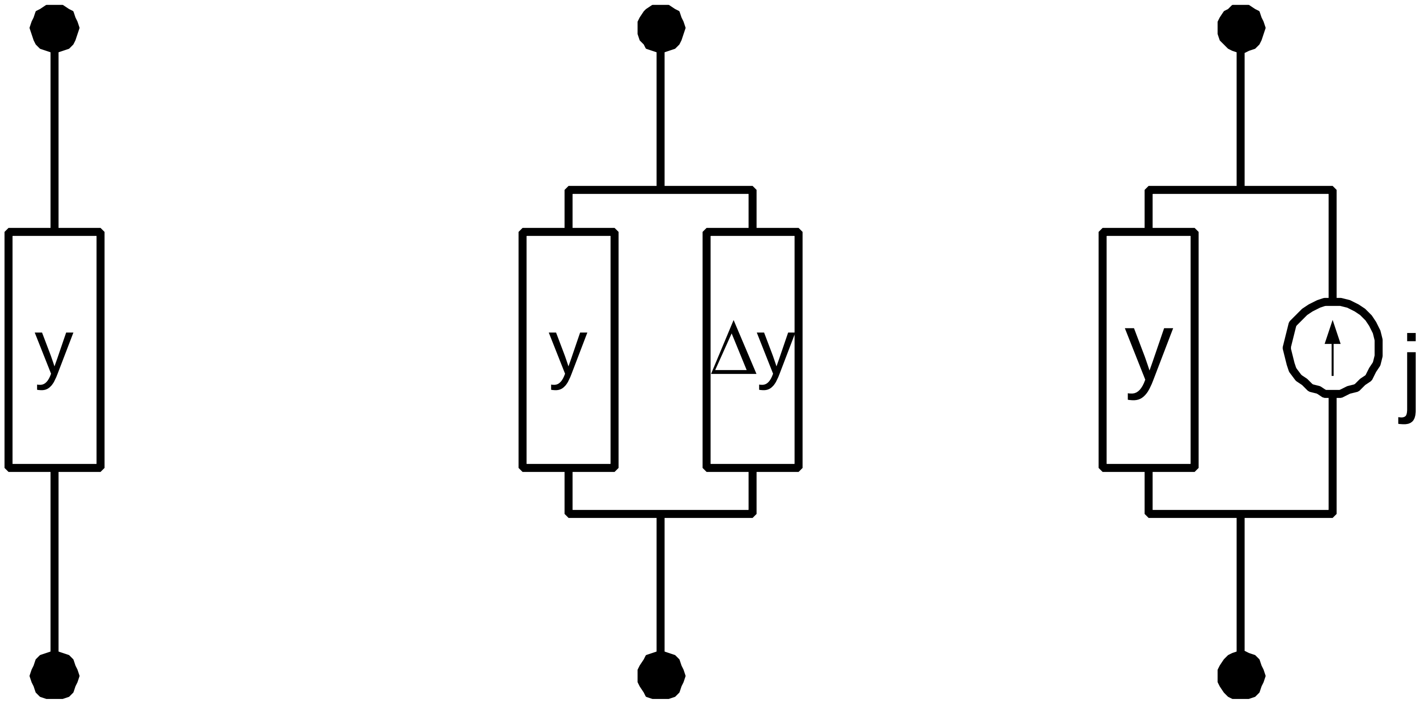
1) If $R_1 = R_2$ then $V_{out} = 0.5 \cdot V_{in}$;

2) When the parameter of resistor R_2 deviates on 15 % from its nominal value, then $V_{out} \approx 0.53 \cdot V_{in}$;

3) When the parameter of resistor R_1 deviates on 15 % and resistor R_2 on 10 %, then $V_{out} \approx 0.49 \cdot V_{in}$

The faults of the analog circuits:

Models of Parametric fault



Nominal Admittance

Actual Admittance

The Compensation Model

The faults of the analog circuits:

The kinds of catastrophic faults:

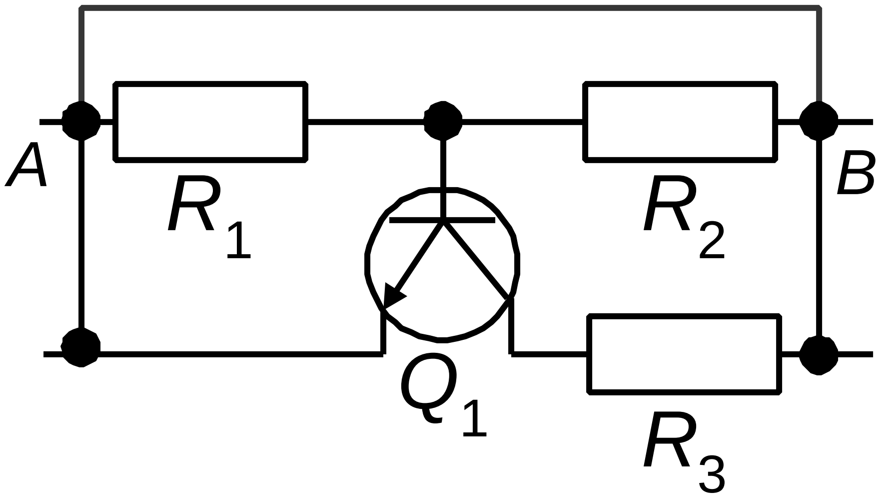
- ***Shorts*** } (either PCB's routes
- ***Opens*** } or conducting paths of IC)
- ***Physical element destruction***

(thermal breakdown or mechanical damage)

The faults of the analog circuits:

Shorts

They arise due to additional conducting paths which connect two or more nodes of the circuit together.



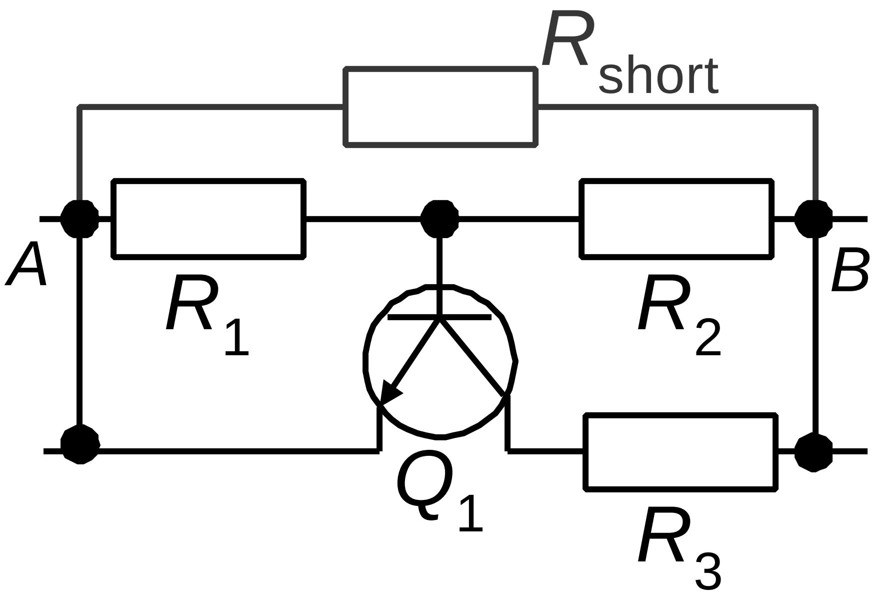
<u>The reasons of arising:</u>

1) In **IC** as a result of conducting paths contact among themselves or with package, or as a result of local overheating and fusing of overheated place;

2) In **PCB** in case of inaccurate mounting, when a drop of solder bridges some connecting lines (routes).

The faults of the analog circuits:

The modeling of shorts on schematic level

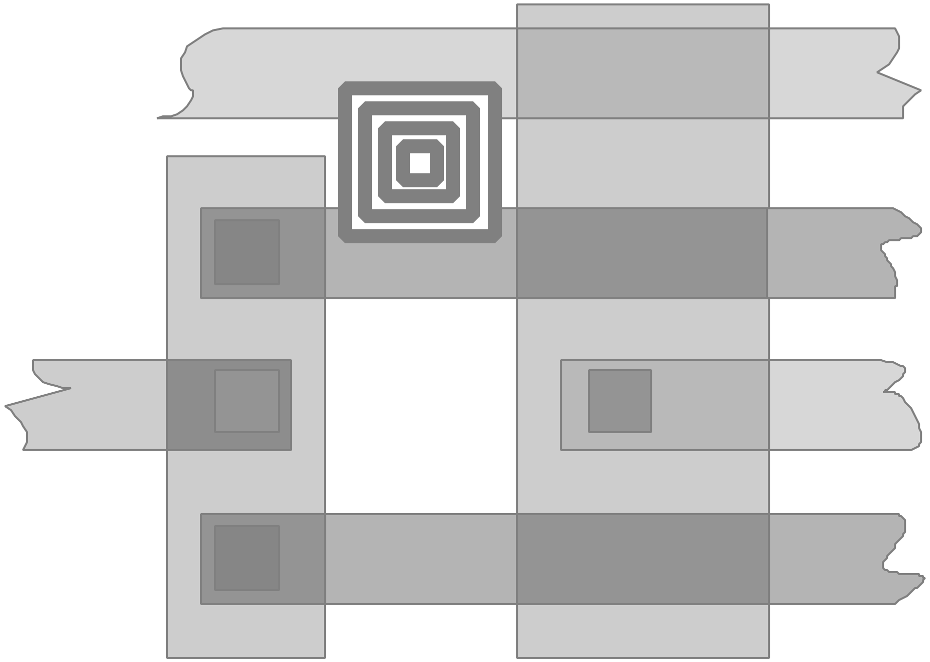


That modeling can be carried out by simple insertion of a resistor R_{short} between two nodes. The insertion process can be repeated for all combinations of two nodes.

The value of used resistor must be sufficiently small and is selected usually from the range from 1 up to 10 Ohm.

The faults of the analog circuits:

The modeling of shorts on topological level

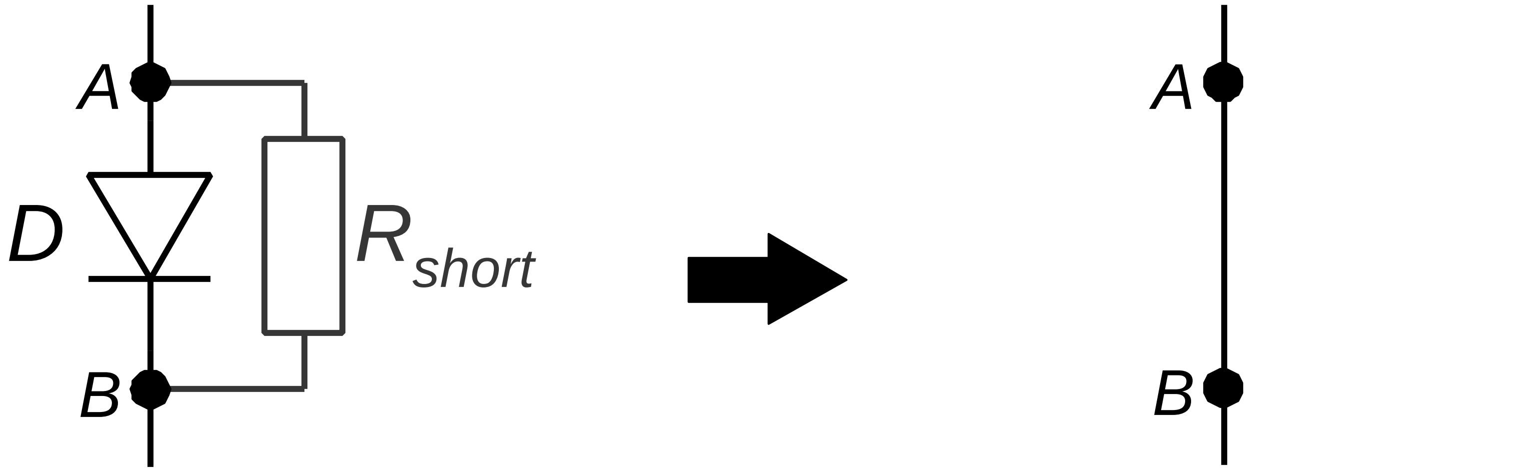


The faults are generated here randomly on a layout of IC as conductive square of defined size and plane geometry.

The basic disadvantage of this approach, which limits its usage, is the requirement of information about silicon and physical layout.

The faults of the analog circuits:

Examples of short influences on analog device functioning

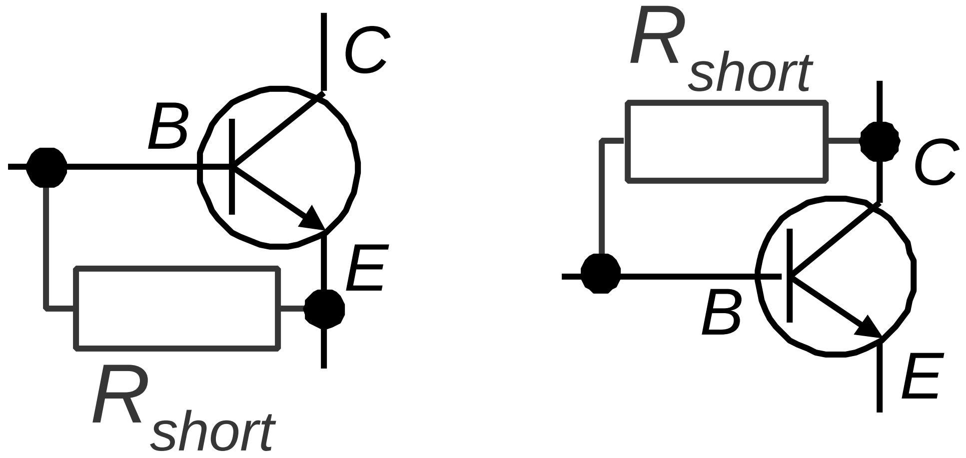


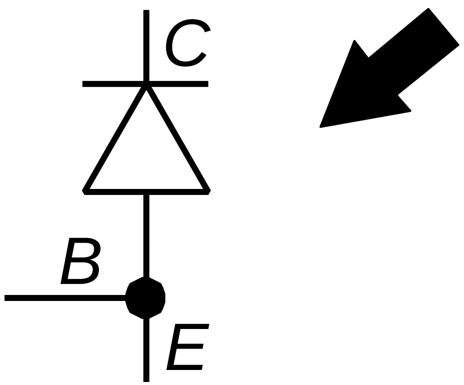
Diode under short

A simple conductor

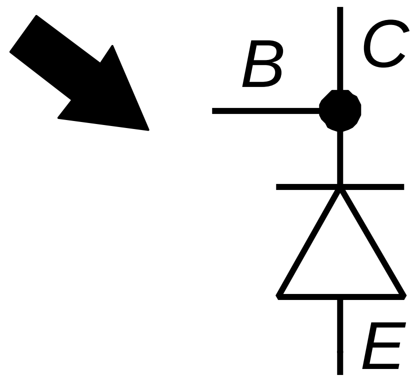
The faults of the analog circuits:

Examples of short influences on analog device functioning





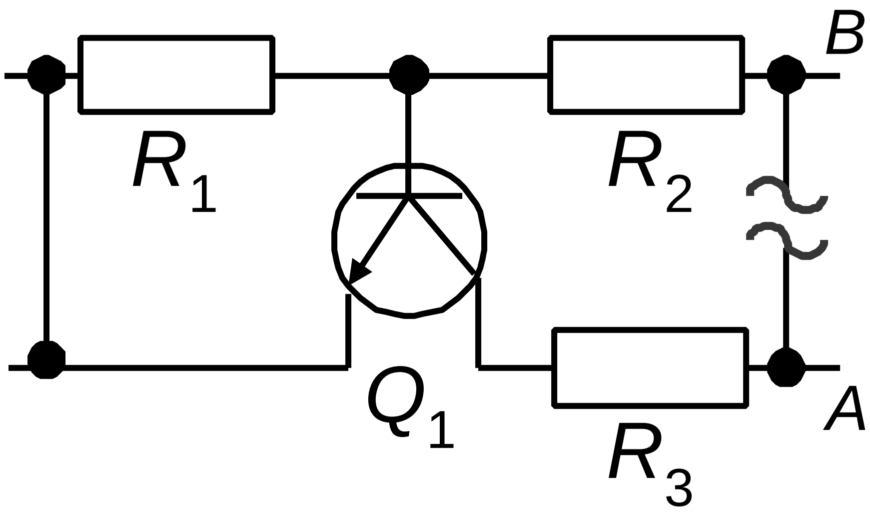
Bipolar transistor under short works like a semiconductor diode



The faults of the analog circuits:

Opens

They occur in conducting paths of ICs or connected lines of PCBs as the missing sections of them.



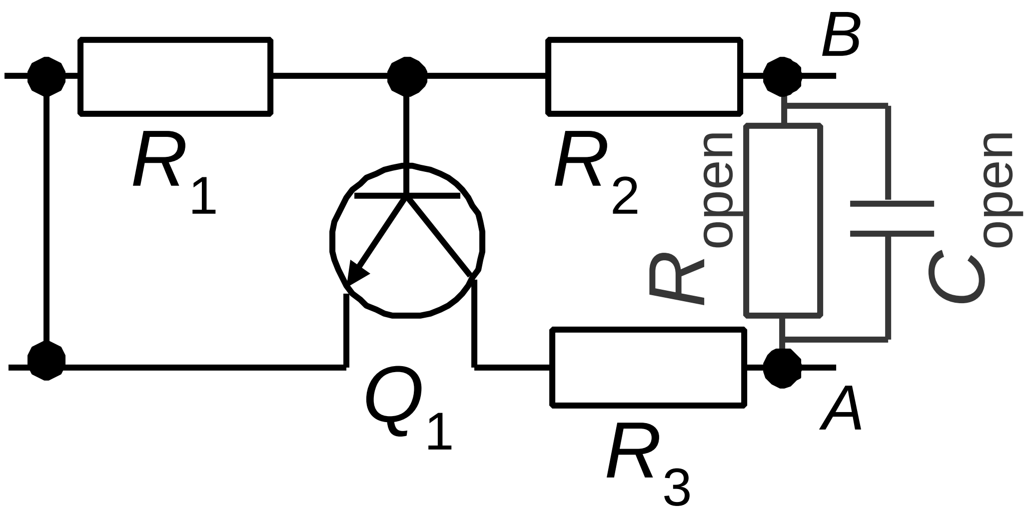
The reasons of arising:

1) In **IC** due to both mechanical influences and in result of electrochemical and chemical processes.

2) In **PCB** are caused by poor-quality solder of electronic devices contacts to board bonding contact pads and by physical destruction.

The faults of the analog circuits:

The modeling of opens on schematic level

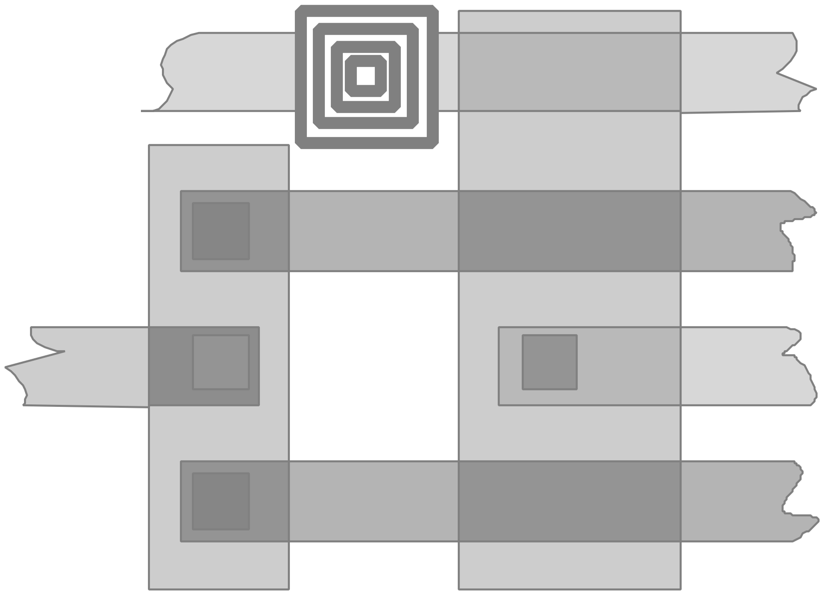


A resistor of high value and capacitor are used for modeling, which are connected up in parallel between component electrode on the one hand and circuit node on the other hand.

The resistor value is selected from the range from 10MOhm up to 100MOhm, and values of capacitor lie in the range from 0.1fF up to 1fF.

The faults of the analog circuits:

The modeling of opens on topological level

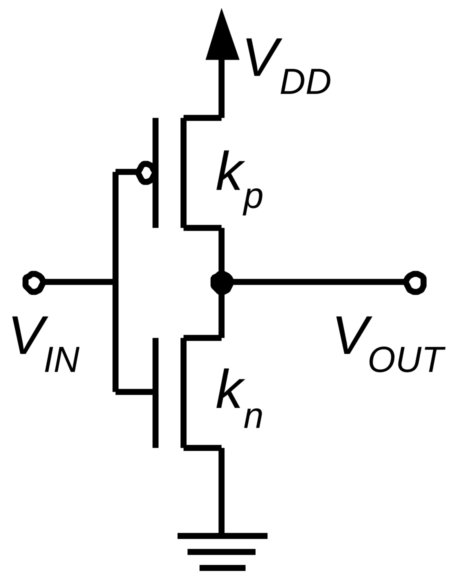


The faults are generated here randomly as a square of defined size and plane geometry, which breaks conductivity in the layer of IC.

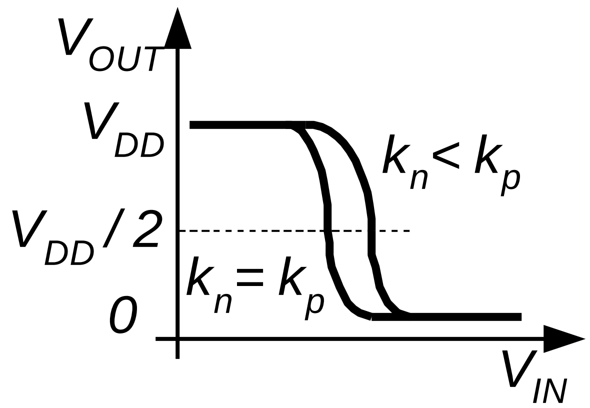
If such square falls on the conductive path, then the path is considered as broken.

The faults of the analog circuits:

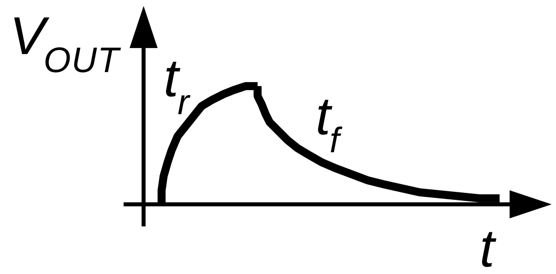
CMOS inverter circuit



Digital circuit of inverter on two CMOS transistors



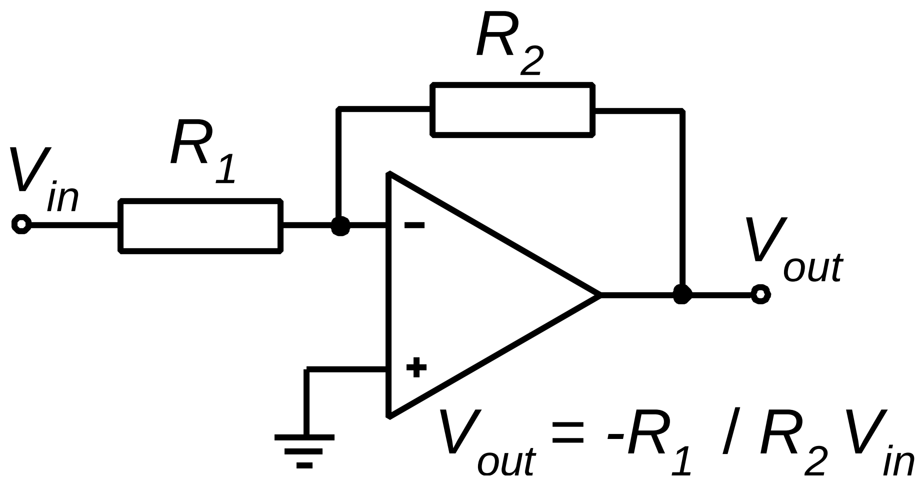
DC transfer characteristic



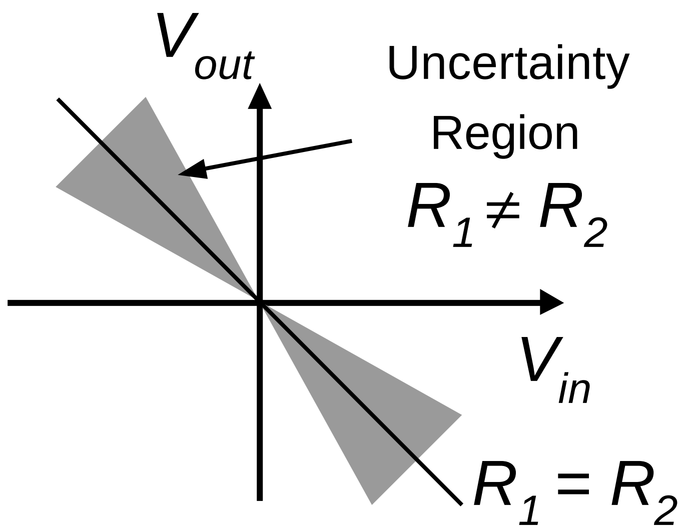
Pulse characteristic

The faults of the analog circuits:

OpAmp inverter circuit



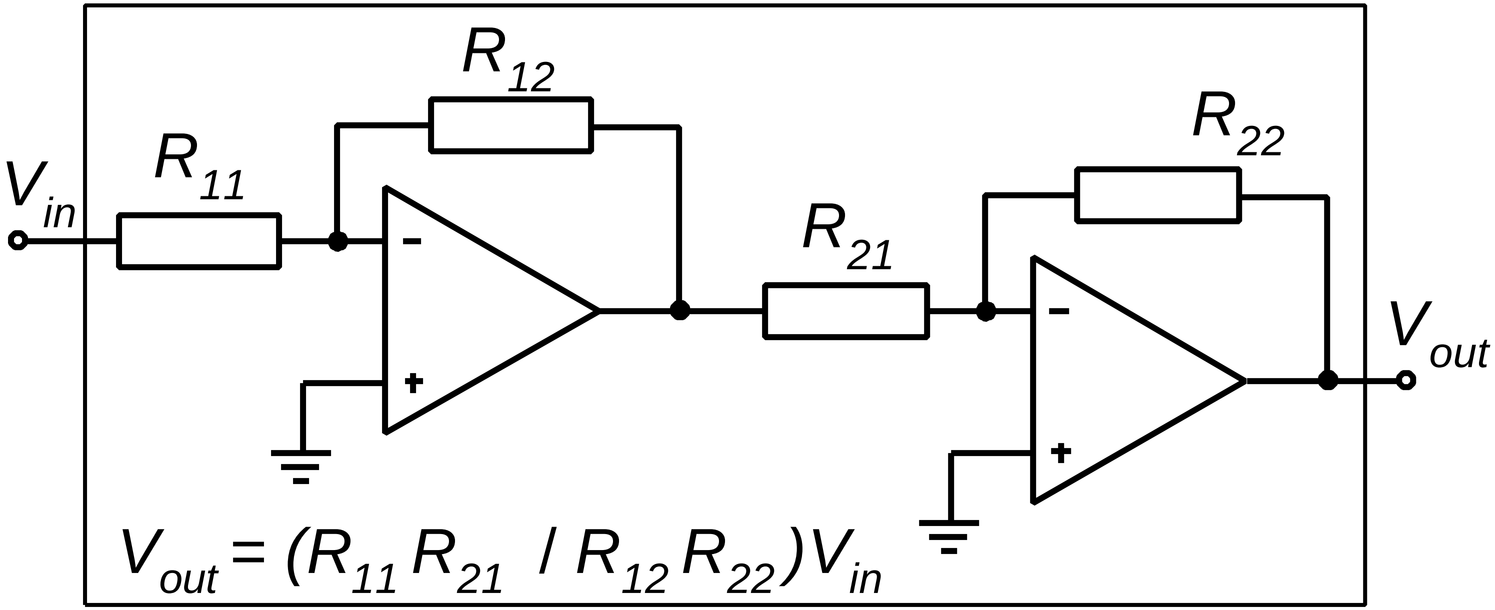
Analog circuit of inverter on Operational Amplifier



DC transfer characteristic

The faults of the analog circuits:

An example of unessential contribution of mismatch errors on violation of circuit's operation



if Actual $Gain_1$ = - 0.7 (Error consists of 30 %) and

Actual $Gain_2$ = - 1.4 (Error consists of 40 %)

then Actual $Gain_{1\&2}$ = 0.98 (Error consists of 2 %)

The faults of the analog circuits:

Description of analog circuit function

Difficulties:

- Continuous character of analog processes;
- Complex nonlinear relation between input and output signals.

The notation of analog circuit function is performed on the base of Kirchhoff's and Ohm's laws, which define association between electrical current and voltages in circuit.

The faults of the analog circuits:

Description of analog circuit function

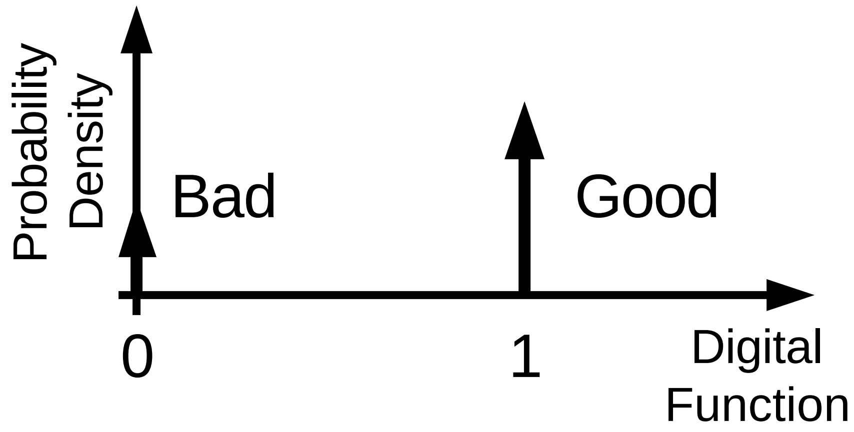
For simulation analog function is brought to different equations set (linear, nonlinear, differential) of several variables, solution of which is possible only with some precision.

Main results of analog circuit simulation:

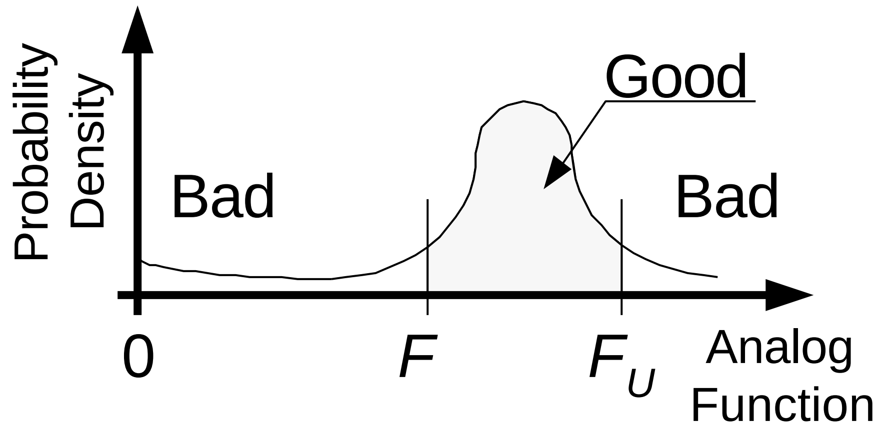
- Estimation of circuit nominal operation;
- Definition of uncertainty region for output characteristics.

The faults of the analog circuits:

Differences between functioning of analog and digital circuits



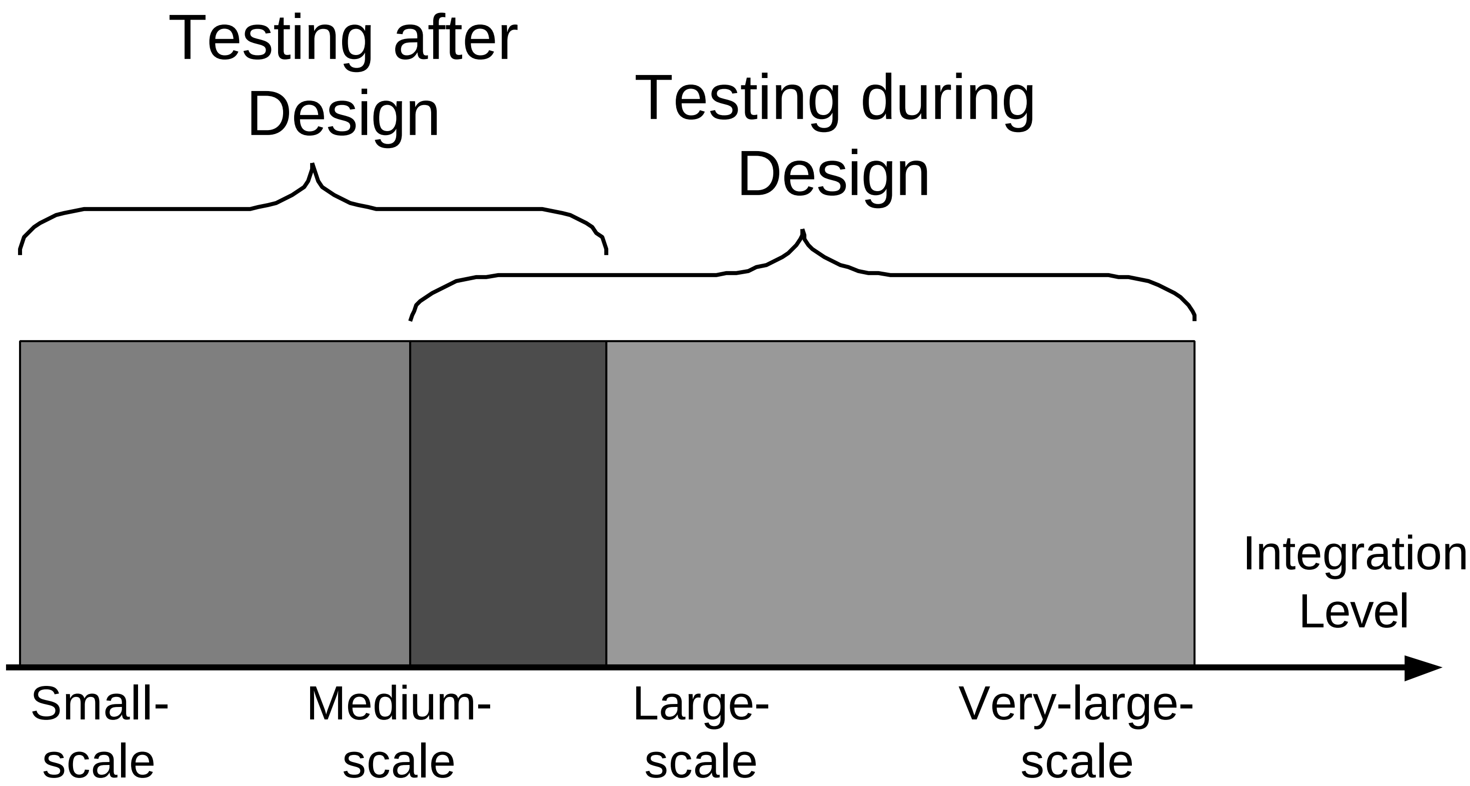
Estimated probability of faults in digital circuit



Estimated probability of faults in analog circuit

Testability measuring:

The strategies of testing



Testability measuring:

A quantitative estimation
of analog circuit testability

Enumerable methods	Algorithmic methods
+ Simplicity of realization; + Estimation of various design and technological solutions influences; - Crude estimation of a testability.	+ Qualitative estimation based on the circuit's topological description; + Detection of areas with low testability; - High computational expenses.

Testability measuring:

Characteristics of analog circuit testability

For internal nodes:

Controllability is understood as relative difficulty of setting a node to a specific value.

Observability is understood as relative difficulty of propagating an error from an internal node to a primary output.

Testability measuring:

Characteristics of analog circuit testability

For internal components:

Testability Transfer Factor (TTF) allows to determine how controllability and observability influence on passing of test information, which is propagated through one components to other components or to primary outputs.

Testability measuring:

Controllability

This measure is normalized to range between 0.0 and 1.0, with 1.0 being totally controllable and 0.0 being totally uncontrollable.

Primary inputs are by definition totally controllable.

Testability measuring:

Observability

This measure is normalized to range between 0.0 and 1.0, with 1.0 being totally observable and 0.0 being totally unobservable.

Primary outputs are by definition totally observable.

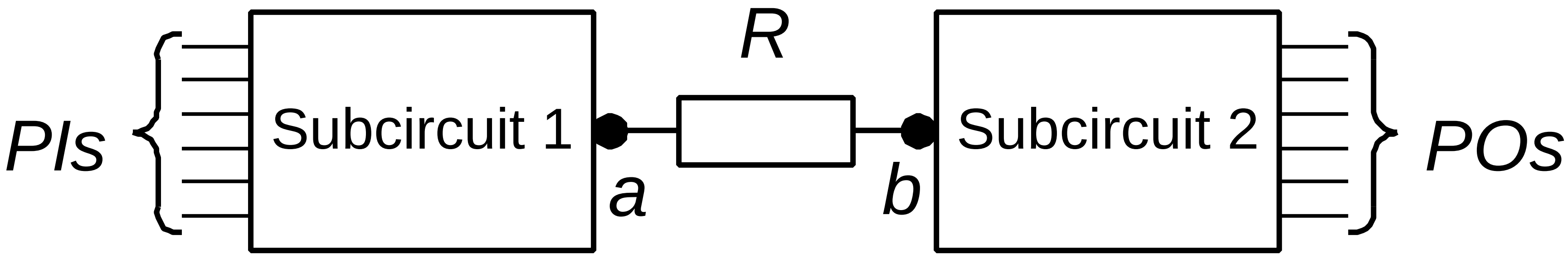
Testability measuring:

Testability Transfer Factor

The ***TTF*** of component represents, firstly, easiness of achieving an arbitrary signal on its outputs by exercising its inputs, and secondly, easiness of determining whether a specific signal occurred on its inputs by examining the values on its outputs.

Testability measuring:

Testability Transfer Factor calculation for passive components



Node *b* in that circuit is controllable by node *a* only if a current of magnitude *I* can flow from node *a* to node *b*. The current *I* is described by Ohm's law as:

$$I = \frac{V_a - V_b}{R} \quad .$$

Testability measuring:

Testability Transfer Factor calculation for passive components

Node ***b*** is **totally controllable** by node ***a*** if *R* is equal to zero (short circuit) and is **totally uncontrollable** by node ***a*** if *R* is equal to infinity.

Similarly, node ***a*** is **totally observable** by node ***b*** if *R* is equal to zero, and node ***a*** is **unobservable** by node ***b*** if *R* is equal to infinity

Testability measuring:

Testability Transfer Factor calculation for passive components

Such dependence can be expressed quantitatively in the form of equation for resistor's ***testability transfer factor*** as

$$T_f(R) = 1 - \frac{R}{OC}$$

where $T_f(R)$ is TTF for resistor R; R is a real value of resistor; OC is a resistance, which provides open-circuit condition.

Testability measuring:

Testability Transfer Factor calculation for passive components

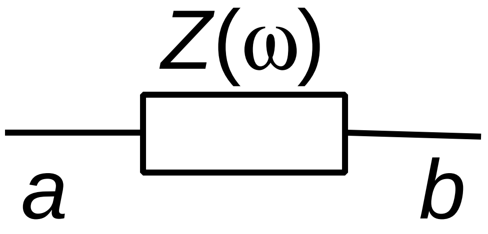
Capacitors and ***inductors*** may be modeled as frequency-dependent resistors. Therefore expression for evaluation of passive components TTF can be shown as

$$T_f(R) = 1 - \frac{Z(\omega)}{OC}$$

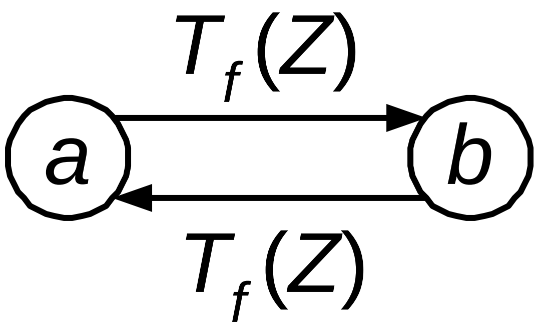
where Z is a full resistance of component, and ω is a frequency.

Testability measuring:

Signal Flow Graph (SFG) for electronic components



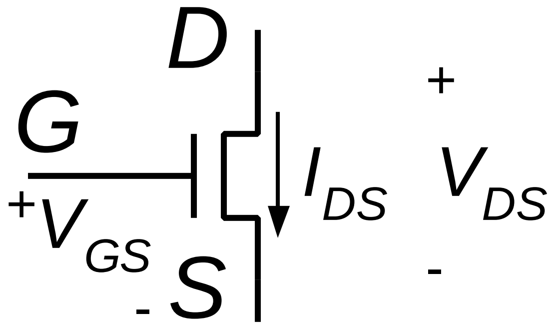
Each circuit component can be represented by graph-based model, which reflects the internal signals flows.



The vertexes of the given graph correspond to a nodes of component connection, and edges correspond to paths of signals propagation through component. The weight of each edge is the TTF value of the component.

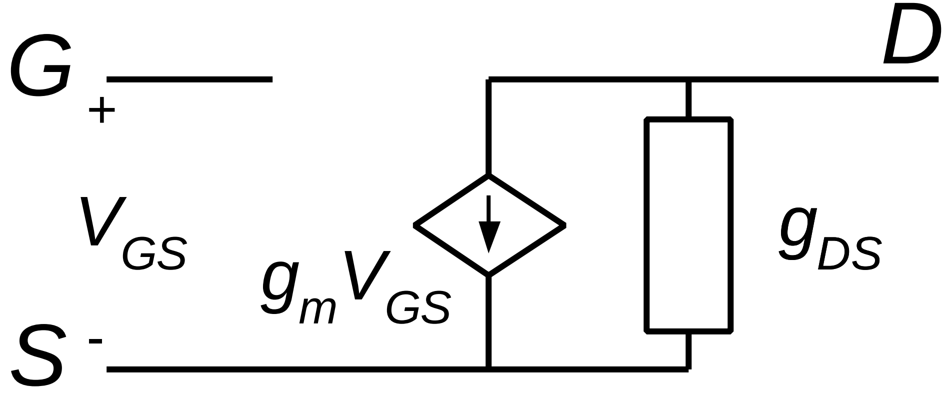
Testability measuring:

TTF calculation for MOSFET transistor



$$I_{DS} = f\left(V_{GS},\ V_{DS}\right)$$

Symbolic notation of n-type MOSFET



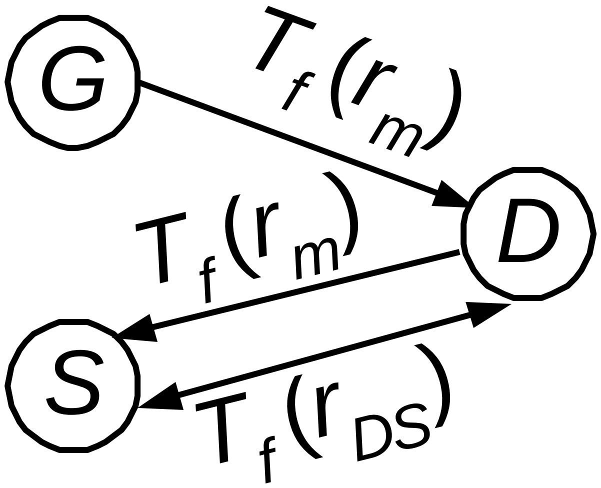
$$g_m = \frac{\partial I_{DS}}{\partial U_{GS}} = \frac{1}{r_m}\ ;\ g_{DS} = \frac{\partial I_{DS}}{\partial U_{DS}} = \frac{1}{r_{DS}}$$

Equivalent circuit for the MOSFET

Testability measuring:

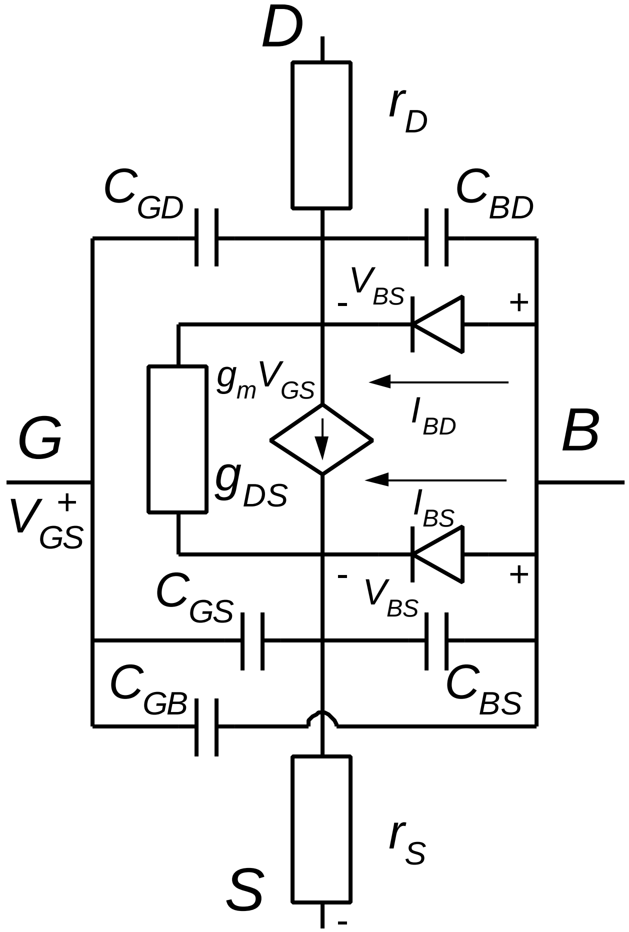
TTF calculation for MOSFET transistor

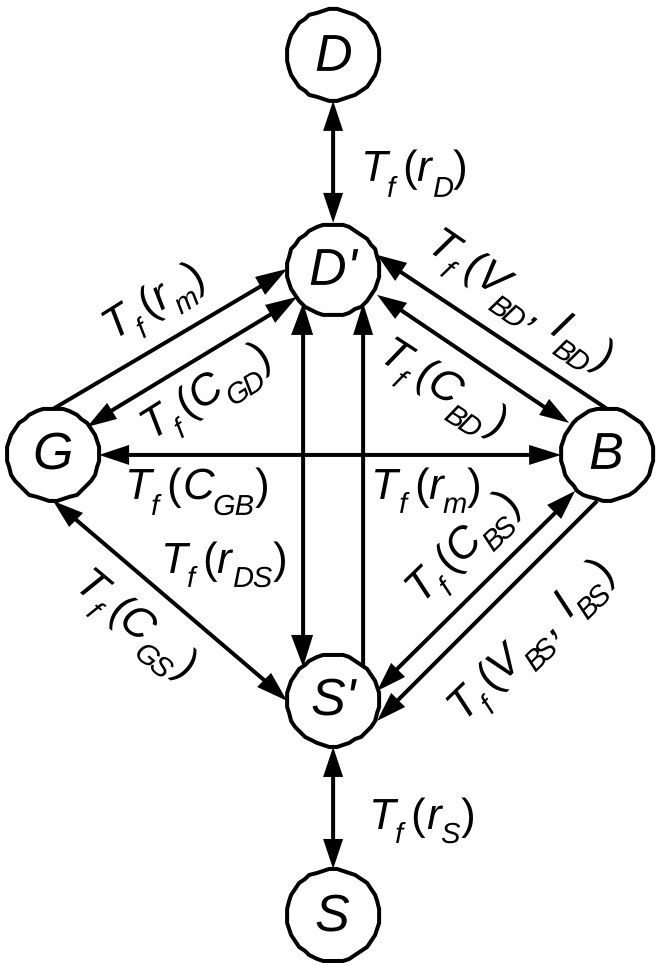
Resistors r_m and r_{DS} are used for TTF calculation for everyone model components. Obtained values of TTF are used as weights at appropriate edges of the signal flow graph for simplified MOSFET's model.



Testability measuring:

Advanced MOSFET model and SFG for it





Testability measuring:

Controllability calculation

The ***input controllability*** of a component represents the easiness of achieving an arbitrary signal value at the component's inputs.

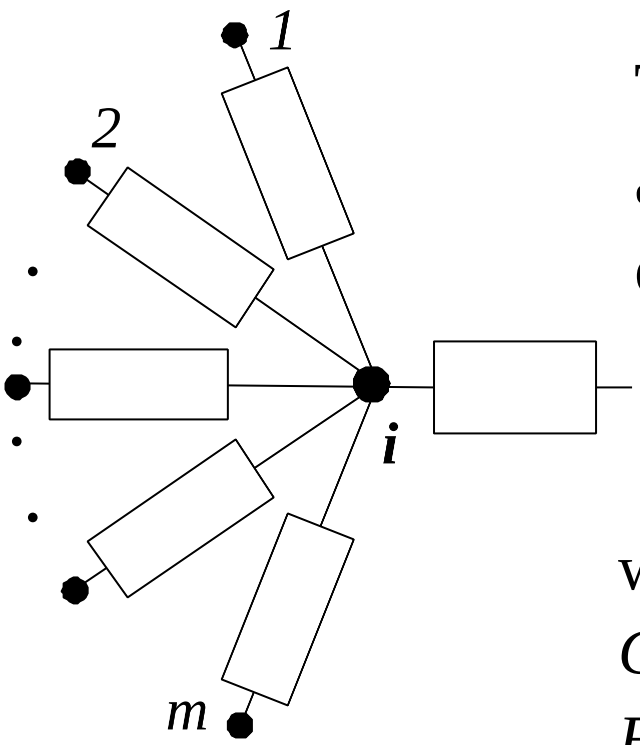
The ***output controllability*** of a component represents the easiness of producing an arbitrary signal value on the outputs of the component. It depends on the input controllability and the testability transfer factor of the component

$$C_{out} = T_f C_{in}$$

where C_{in} – input controllability of the component;
C_{out} – output controllability of the component;
T_f – Testability Transfer Factor of the component.

Testability measuring:

Controllability calculation



The ***controllability*** for any node ***i*** (or any vertex *i* in the signal flow graph) can be expressed as

$$C_i = \frac{1}{F_{in}} \sum_{m=1}^{F_{in}} C_m \left(T_f\right)_m ,$$

where

C_i – controllability of node ***i***;

F_{in} – fan-in of node ***i***;

C_m – controllability at source node of fan-in *m*;

$\left(T_f\right)_m$ – Testability Transfer Factor of fan-in *m*.

Testability measuring:

Observability calculation

The ***output observability*** of a component represents the easiness of determining whether or not the expected signal value occurs at the inputs of the component by observing the signal values at the primary outputs of the circuit.

The ***input observability*** of a component represents the easiness of determining whether or not the expected signal value occurs there, by observing the signal values at the primary outputs of the circuit.

Testability measuring:

Observability calculation

Since the testability transfer factor represents the easiness of propagating a signal through the component, then ***input observability*** can be expressed as

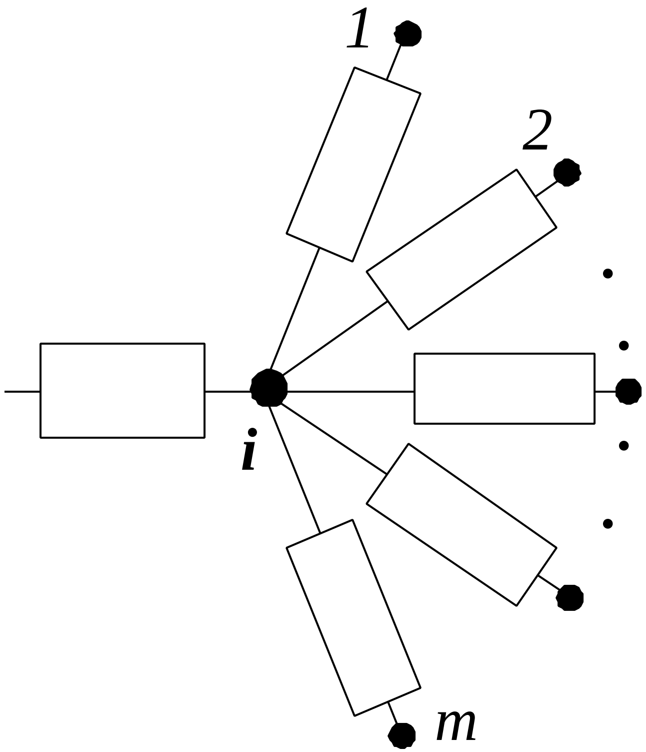
$$O_{in} = T_f O_{out} \quad ,$$

where

O_{in} – input observability of the component;
O_{out} – output observability of the component;
T_f – Testability Transfer Factor of the component.

Testability measuring:

Observability calculation



The ***observability*** for any node ***i*** (or any vertex *i* in the signal flow graph) can be expressed as

$$O_i = \frac{1}{F_{out}} \sum_{m=1}^{F_{out}} O_m \left(T_f\right)_m \quad ,$$

where

O_i – observability of node ***i***;

F_{out} – fan-out of node ***i***;

O_m – observability at source node of fan-out *m*;

$\left(T_f\right)_m$ – Testability Transfer Factor of fan-out *m*.

Testability measuring:

Testability calculation

For ***testability measure*** of circuit node ***i*** the geometric mean of two characteristics (controllability and observability) are proposed to use:

$$T_i = \sqrt{C_i \cdot O_i} \quad ,$$

where

T_i is the testability of node ***i***;
C_i is the controllability of node ***i***;
O_i is the observability of node ***i***.

Testability measuring:

Testability calculation

The common testability measure of a whole circuit can be expressed as simple mean value of testability measures of all circuit nodes:

$$T = \frac{\sum_{i=1}^{N} T_i}{N} ,$$

where

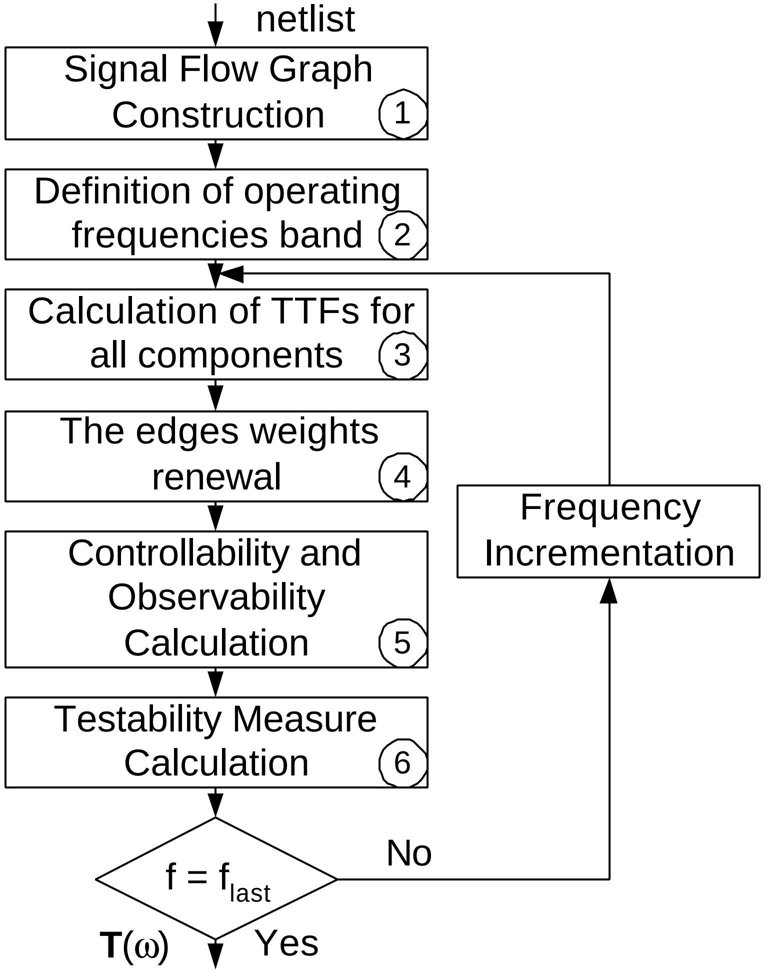
T is the testability of a circuit;

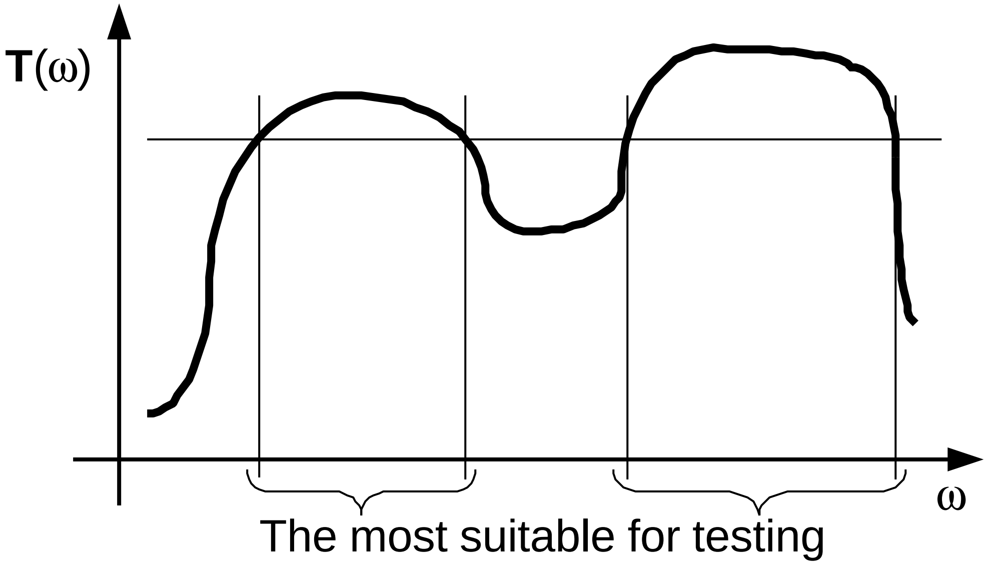
T_i is the testability of node ***i***;

N is a number of circuit nodes.

Testability measuring:

The Algorithm of a Testability calculation





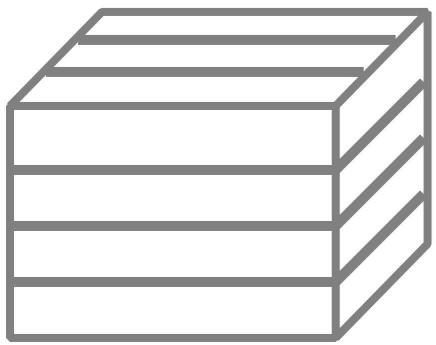
The function of testability depending from frequency of input signal

The approaches of analog circuit testing:

Analog Testing

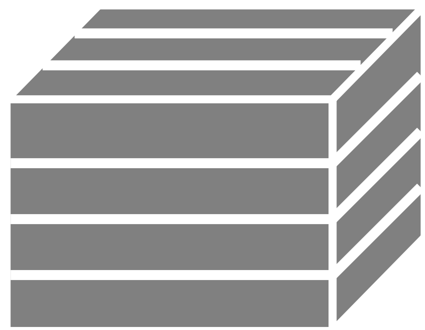
Structural

Consideration of a tested circuit as a "White Box"



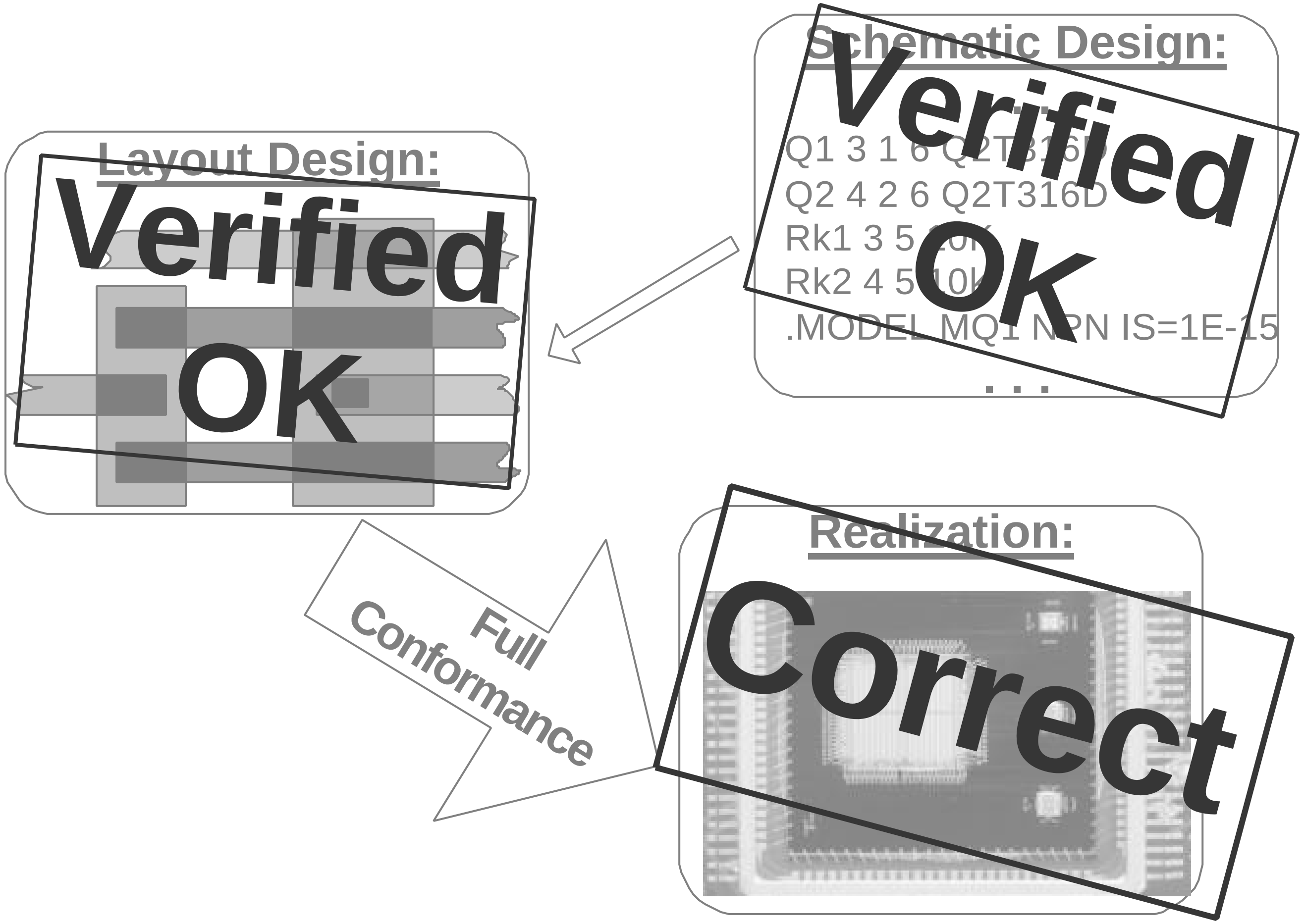
Functional

Consideration of a tested circuit as a "Black Box"



The approaches of analog circuit testing:

Structural Testing



The approaches of analog circuit testing:

Functional Testing

The main advantages:

- Simplicity of test signal selection during a design stage of devices;
- Support of checking of the output characteristics correspondence to their technical specifications;
- Allows to make fault diagnosis;
- Easiness of integration with methods of digital circuits functional testing, etc.

The approaches of analog circuit testing:

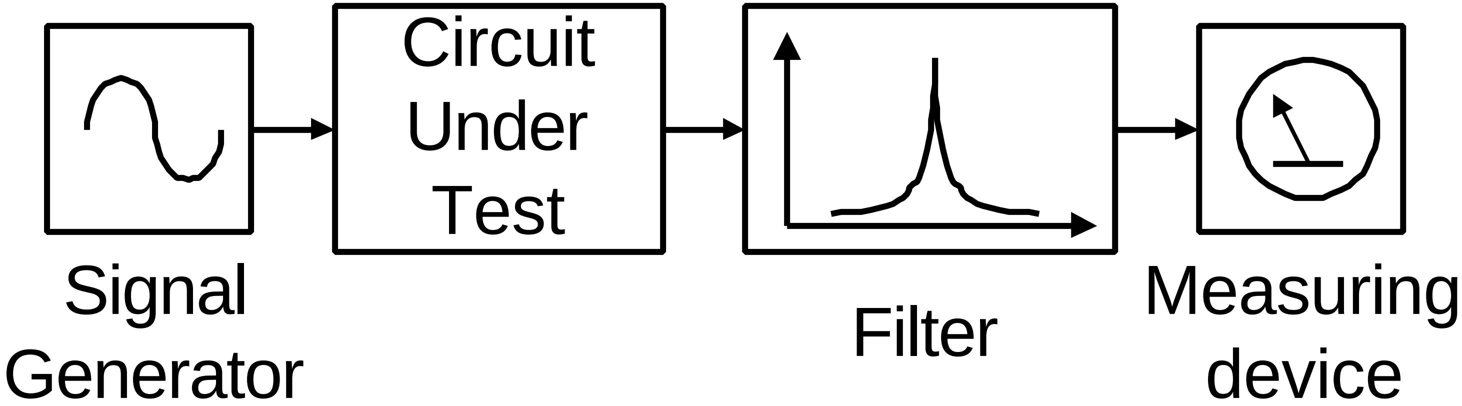
Functional Testing

Disadvantages:

- Difficulties to write test programs;
- High dimensions of test vectors for the large circuits;
- High computing expenses, etc.

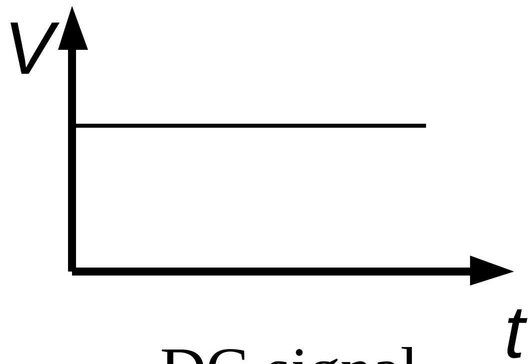
The approaches of analog circuit testing:

Typical structure of analog test setup

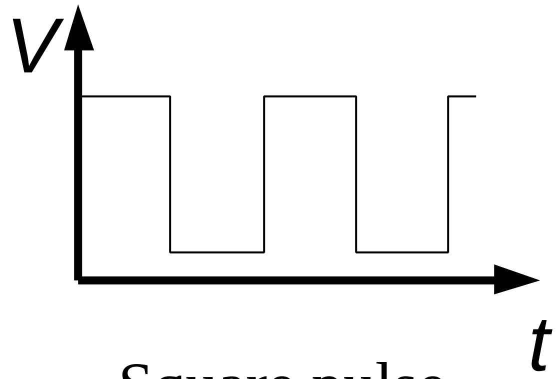


The approaches of analog circuit testing:

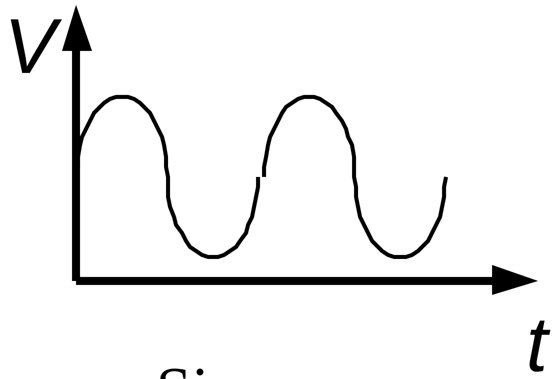
The waveform of excited signals



DC signal



Square pulse



Sine wave

Special form

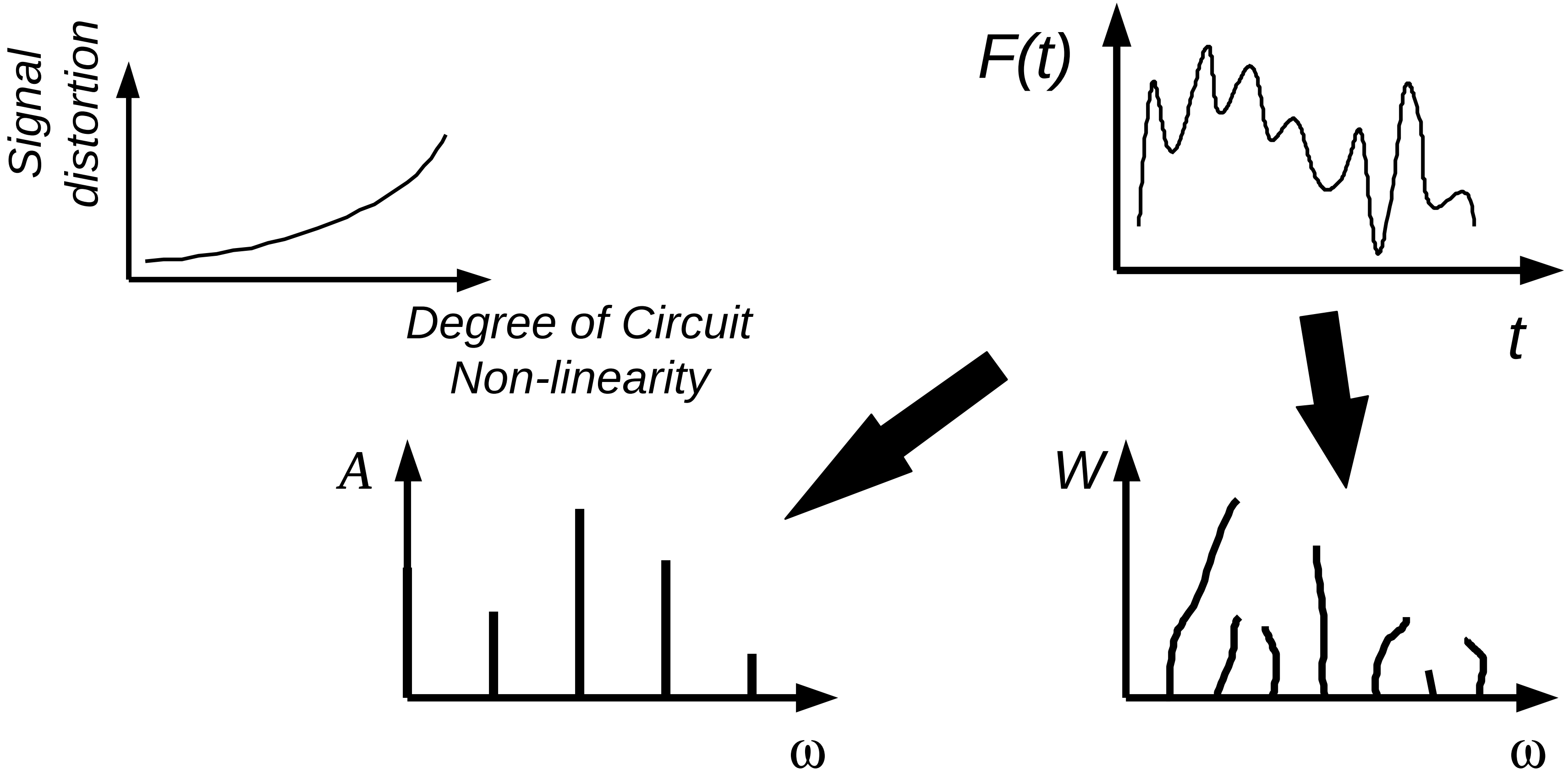
The approaches of analog circuit testing:

Main measurement categories

- ***DC measurements*** (static mode);
- ***AC measurements*** (frequency domain);
- ***Transient measurements*** (time domain);
- ***Noise measurements***.

The approaches of analog circuit testing:

The influence of non-linearity



Fourier Transform Wavelet-analysis

Functional Diagnosis:

Approaches of analog circuits functional diagnosis

SBT
(*simulation before testing*)

SAT
(*simulation after testing*)

Functional Diagnosis:

The general algorithm of SBT functional diagnosis

- Generation of the faults list;
- Obtaining output responses of device for these faults;
- Creation of the fault dictionary ;
- Measurement of CUT's output responses on test signals;
- Comparison of obtained responses of the CUT with values from the fault dictionary and decisionmaking about circuit correctness.

Functional Diagnosis:

Main problems of fault dictionaries usage

- ***High dimensions.*** The inclusion of large number of output responses results in large expenses of resources;
- ***Limitations of a set of saved output responses.*** That do not allow to diagnose the faults which have not been included in the fault dictionary.

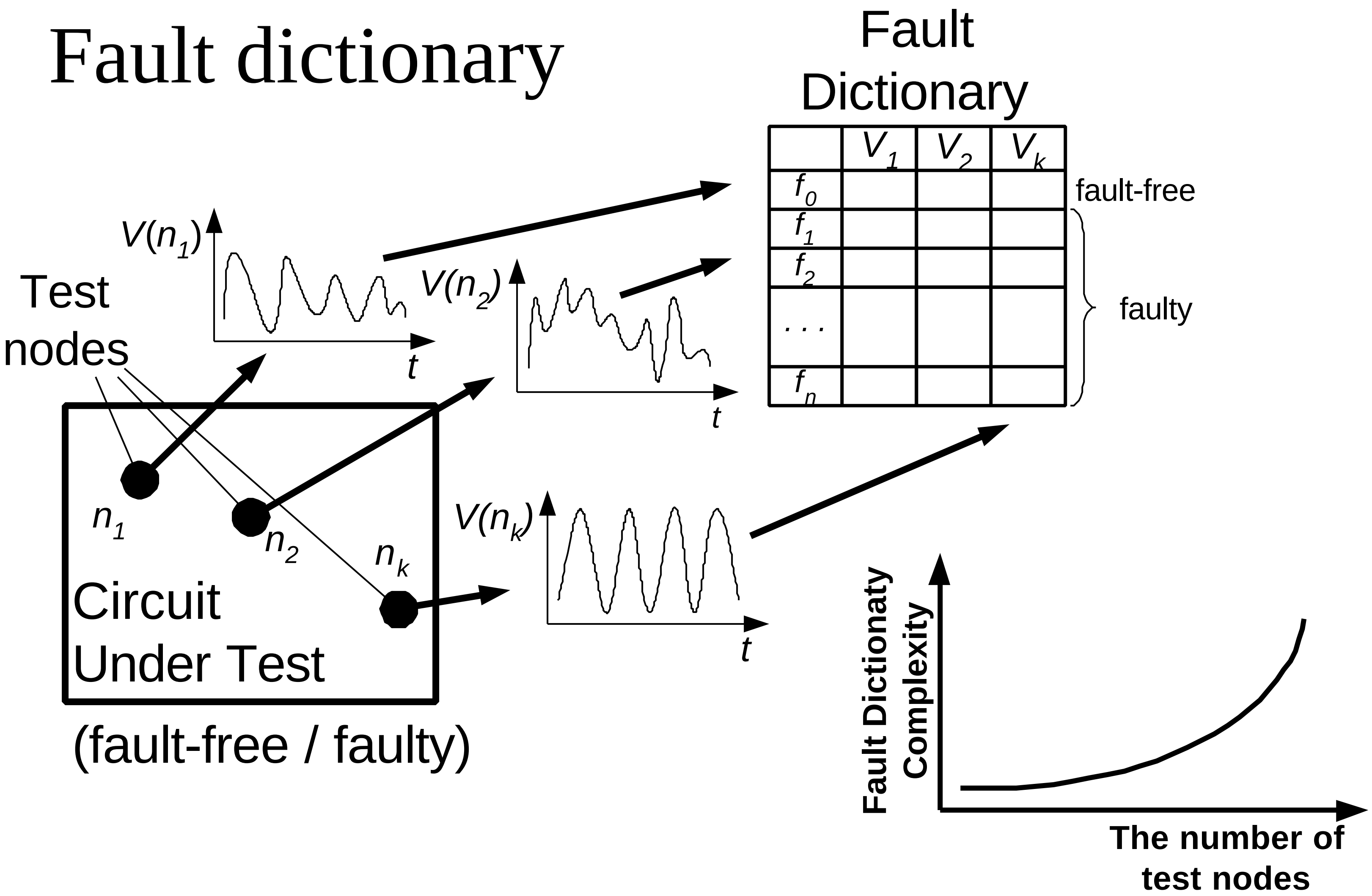
Functional Diagnosis:

The approaches of fault dictionary construction

- *Methods of DC models;*
- *Methods of models at frequency domain;*
- *Methods of models in time domain.*

Functional Diagnosis:

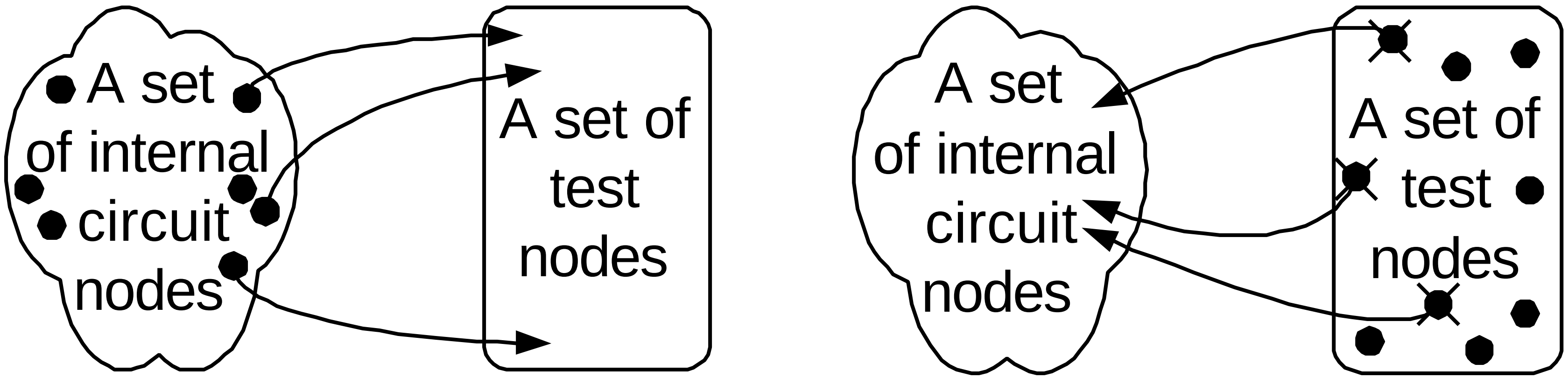
Fault dictionary



Functional Diagnosis:

Strategies of Test Nodes Selection

Including selection | **Excluding selection**



Functional Diagnosis:

The role of Ambiguity Group

For solution of the diagnosis task the important moment at a selection of test nodes is reduction of the number and cardinality of ambiguity groups.

Ambiguity group is understood as a set of faults, the influence of which on the measured value at defined input test signals are identical.

Functional Diagnosis:

Tabular- and Entropy-based method for test nodes selection

Fault-wise table

$\boldsymbol{C} =$

	n_1	n_2	n_3	. . .	n_k	
f_0	1	7	7		1	fault-free
f_1	1	12	1		6	faulty
f_2	3	5	2		3	faulty
. . .						faulty
f_n	10	1	5		3	faulty

For each test node the finite set of ambiguity groups is formed. This groups are numbered from 1 up to m_p, where m_p is cardinality of this set for test node p.

Each cell of the fault-wise table C_{ij} contains the number of ambiguity group generated for node j and fault i.

Functional Diagnosis:

Tabular- and Entropy-based method for test nodes selection

$F = \{ f_0, f_1, \ldots, f_k \}$ is a subset of all possible faults F;

$N = \{ n_1,\ n_2, \ldots,\ n_p \}$ is the subset of all test nodes N.

Let $C_j = \{ C_{kj} \in C \}$ is a subset of fault-wise table C connected to test node n_j. If $C_{mj} \neq C_{nj}$ for each pair (C_{mj}, C_{nj}), where $C_{mj} \in C_j$ and, $C_{nj} \in C_j$ $(m \neq n)$ the system is completely diagnosed with use of a node n_j.

Functional Diagnosis:

Tabular- and Entropy-based method for test nodes selection

When $C_{mj} = C_{nj}$ for $(m \neq n)$, the appropriate faults f_m and f_n belong to ambiguity group connected to test node n_j , which can be defined as $F_{ij} = \left\{ f_m \in F \Big|_{a_{jm}=i} \right\}$.

The analog circuit is completely diagnosable for a set of test nodes N_f, if for each fault i $(i \neq j)$ there is such node k $\left(\exists k \in N_f,\ N_f \subset N\right)$, that $C_{ik} \neq C_{jk}$.

Functional Diagnosis:

Tabular- and Entropy-based method for test nodes selection

Let X_{ij} ($i = 1, 2,..., k$) is number of elements in ambiguity group F_{ij} for test node n_j. The probability of appearance of a fault from ambiguity group F_{ij} can be calculated as the ratio X_{ij} / X , where $X = k$ is the number of diagnosed faults. Thus, entropy for any selected test node n_j is calculated by the following expression:

$$I_j = -\left[\frac{X_{1j}}{X}\log\left(\frac{X_{1j}}{X}\right) + \frac{X_{2j}}{X}\log\left(\frac{X_{2j}}{X}\right) + \ldots + \frac{X_{kj}}{X}\log\left(\frac{X_{kj}}{X}\right)\right] =$$

$$= \log(X) - \frac{1}{X}\sum_{i=1}^{k} X_{ij}\log(X_{ij})$$

Functional Diagnosis:

Tabular- and Entropy-based method for test nodes selection

Entropy index: $E(j) = \sum_{i=1}^{k} X_{ij} \log(X_{ij})$.

A test node n_j, which minimizes index $E(j)$, guarantees the largest decrease of entropy. The nodes selected in accordance with this criterion constitute the set of test nodes.

Functional Diagnosis:

Algorithm of Tabular- and Entropy-based method for test nodes selection

1. Calculate a number of elements in each ambiguity group for each test node n_j.
2. Calculate the entropy index rate $E(j)$ for all test nodes.
3. Add nodes with minimum value $E(j)$ to the set of selected test nodes.
4. Reform the fault-wise table according to the order of ambiguity groups of a selected test node.

Functional Diagnosis:

Algorithm of Tabular- and Entropy-based method for test nodes selection (continue)

5. Calculate index $E(j)$ for the stayed nodes in view of presence of ambiguity groups at each obtained sub-tables of the fault-wise table.

6. If the index $E(j)$ is equal to zero for all j or if new $E(j)$ has not changed for all j, then the process stops. Otherwise it is necessary to repeat steps 3 - 5.

Example >

Functional Diagnosis:

An example of usage the Tabular- and Entropy-based method for test nodes selection

Table 1. ***The measured voltages in circuit test nodes***

	$V(n_1)$	$V(n_2)$	$V(n_3)$
f_0	3.50	2.80	3.7
f_1	3.50	2.80	4.3
f_2	3.47	2.81	3.0
f_3	3.51	4.20	3.0
f_4	5.00	4.20	4.3

$\{f_0, f_1, f_2, f_3\}$ and $\{f_4\}$ form ambiguity groups for node n_1;
$\{f_0, f_1, f_2\}$ and $\{f_3, f_4\}$ form ambiguity groups for node n_2;
$\{f_0\}$, $\{f_1, f_4\}$ and $\{f_2, f_3\}$ form ambiguity groups for node n_3.

Functional Diagnosis:

An example of usage the Tabular- and Entropy-based method for test nodes selection

For each ambiguity group of each test node a different integer number is assigned to represent the group. So,

ambiguity groups **{f_0, f_1, f_2, f_3}** and **{f_4}** for node n_1 are represented by **1** and **2** respectively;

ambiguity groups **{f_0, f_1, f_2}** and **{f_3, f_4}** for node n_2 are represented by **1** and **2** respectively;

ambiguity groups **{f_0}**, **{f_1, f_4}** and **{f_2, f_3}** for node n_3 are represented by **1**, **2** and **3** respectively.

Functional Diagnosis:

An example of usage the Tabular- and Entropy-based method for test nodes selection

Table 2. ***Fault-wise table***

	n_1	n_2	n_3
f_0	1	1	1
f_1	1	1	2
f_2	1	1	3
f_3	1	2	3
f_4	2	2	2

In each column of the table identical numbers represent the same ambiguity group. However, identical integer numbers in different columns may represent different ambiguity groups.

Functional Diagnosis:

An example of usage the Tabular- and Entropy-based method for test nodes selection

After calculation Entropy Index for nodes n_1, n_2 and n_3 the following values were obtained:

	n_1	n_2	$\boldsymbol{n_3}$
$E(j)$	2.4	2	**1.5**

Node n_3 has minimum value of entropy index $E(j)$. Thus n_3 is the first node, which is located in set of test nodes. As a result of rearrangement, the fault-wise table is divided into three sub-table according to number of ambiguity groups for node n_3.

Functional Diagnosis:

An example of usage the Tabular- and Entropy-based method for test nodes selection

Table 3. ***Rearranged fault-wise table after choosing of node n_3***

	$\boldsymbol{n_3}$	n_1	n_2
f_0	1	1	1
f_1	2	1	1
f_3	2	1	2
f_2	3	1	1
f_4	3	2	2

The circuit condition f_0 is uniquely isolated by measuring the voltage of output signal at node n_3. The row f_0 must be removed from rearranged table.

Functional Diagnosis:

An example of usage the Tabular- and Entropy-based method for test nodes selection

Entropy Index values for partitioned matrix and stayed nodes n_1 and n_2 are:

	n_3	n_1	$\boldsymbol{n_2}$
$E(j)$	-	0.6	**0**

At that the node n_2 has the minimum value of entropy index equal to zero, therefore this node is also located into the set of test nodes and on this step the process of test nodes selection is stopped.
All declared faults can be uniquely diagnosed by voltage measurement of an output signal in two test nodes n_2 and n_3.

Functional Diagnosis:

Neural Network-based methods of functional testing and diagnosis

Advantages:

- Recognition of fault configurations not explicitly included in the training set;
- Neural network trained to recognize single faults can be successfully used to diagnose multiple faults;
- Once trained neural network allows to reduce time of diagnosis;
- Compact representation of fault dictionaries, etc.

Functional Diagnosis:

Neural Network-based methods of functional testing and diagnosis

Disadvantages:

- Large computing and time expenses concerning with Neural Network training;
- Complexity of Neural Network structure selection, etc.

Functional Diagnosis:

Neural Network-based methods of functional testing and diagnosis

Information for NN training

Values of output responses

Syndromes based on the output responses conversion

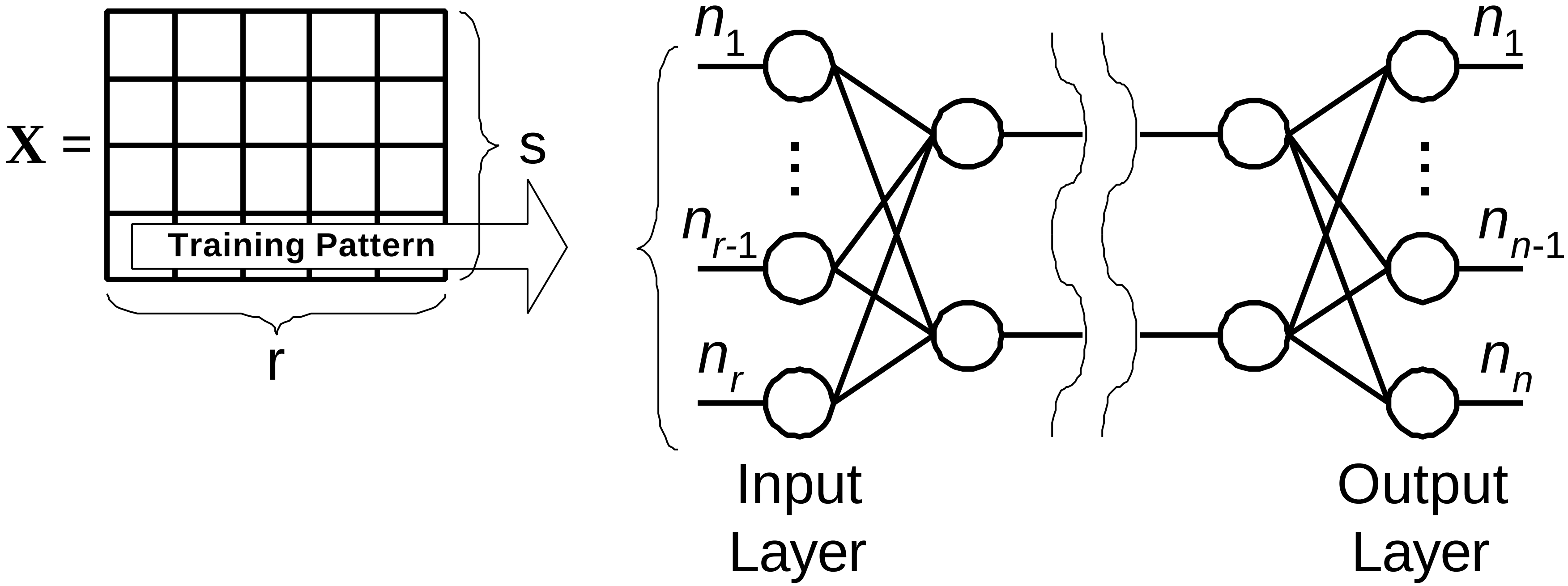
Results of testing with using of NN

Indicator (pass / fail)

A set of "Candidates"

Functional Diagnosis:

Extraction of Essential Features
of analog circuit output signals



Neural Network

Functional Diagnosis:

Extraction of Essential Features of analog circuit output signals

Training input-output patterns

Each pattern is represented by a pair (x_i, y_i), where the vector x_i is ***i***-th row of a matrix X, and the associated vector y_i is defined as follows:

$$y_i(k) = \begin{cases} 0, & \text{if component } k \text{ is not faulty during the } i\text{-}th \text{ acquisition} \\ 1, & \text{if component } k \text{ is faulty during the } i\text{-}th \text{ acquisition} \end{cases}$$

Functional Diagnosis:

The general algorithm of SAT functional diagnosis

- Measuring of circuit under test responses;
- Calculation (estimation) of components parameters with using of circuit output responses and known topological structure;
- Decisionmaking about circuit correctness.

The fault is detected, if one or several estimated component parameters have values outside of tolerance range.

Functional Diagnosis:

The methods of SAT testing and diagnosis

- *The symbolic analysis;*
- *Artificial intelligence systems;*
- *Parametric identification.*

Functional Diagnosis:

The major categories of symbolic methods:

- *Tree enumeration methods;*
- *Flow-graph methods;*

} Topological

- *Numerical interpolation methods;*
- *Parameter extraction methods;*
- *Determinant expansion methods*.

} Algebraic

Functional Diagnosis:

The categories of artificial intelligence approaches:

- *Model-Based Reasoning approach*;
- *Qualitative Reasoning approach*;
- *Fuzzy Logic approach*.

Functional Diagnosis:

Model-Based Reasoning

It works with models describing common structure of the device, its internal components, their interconnections and their correct behaviour. The methods are so effective, as far as the used models are qualitatively described.
A fault here is defined by excluding “anything other than expected behaviour”.

Difficulties:

- Large volume of the used information;
- Complexity, and frequently impossibility, to obtain the required information.

Functional Diagnosis:

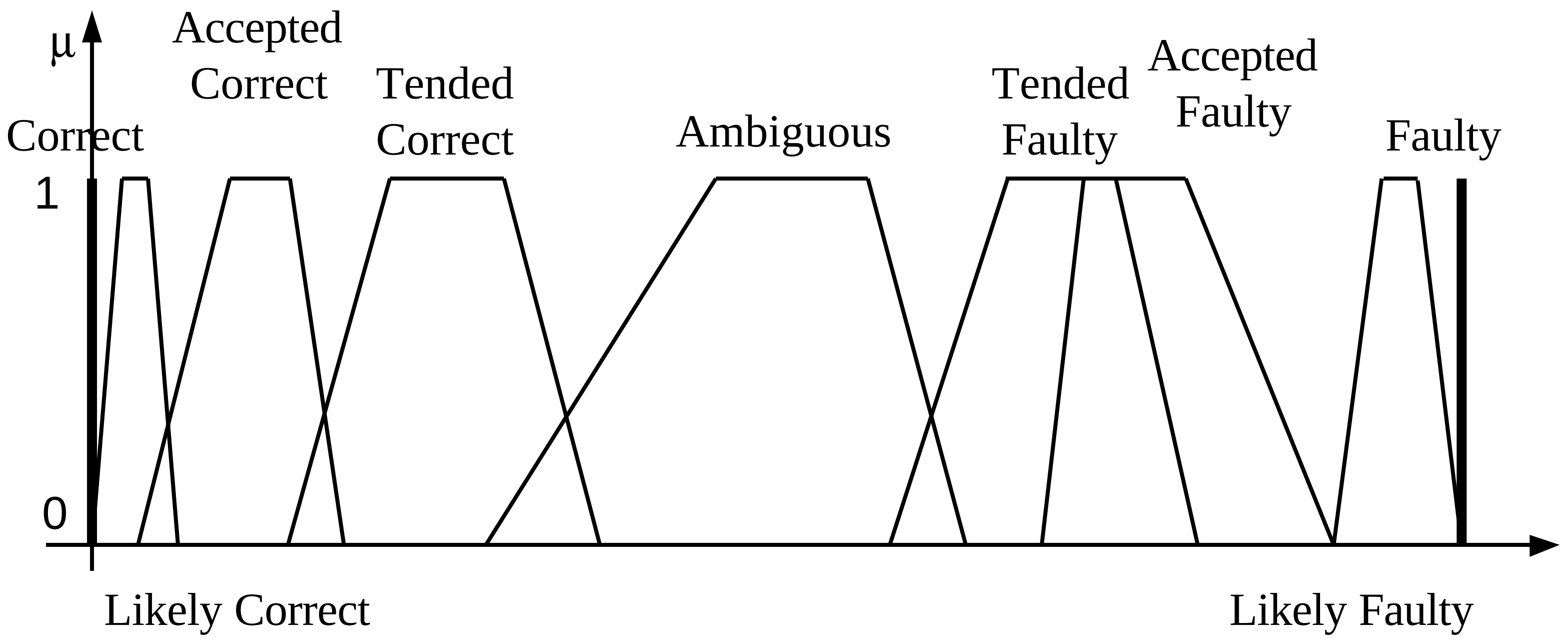
Methods of Qualitative Reasoning

- *Constraint-Centered approach;*
- *Component-Centered approach;*
- *Process-Centered approach.*

The essential difference between the approaches lies in the ontological primitives they use for describing a physical systems.

Functional Diagnosis:

Fuzzy Logic Methods



Fuzzy intervals between correct and faulty operation

Functional Diagnosis:

Parametric Identification

The parametric identification in frame of SAT approach consists in values restoring of circuit component parameters, using for that the values of circuit's output responses at test nodes when test signals are applied to its input.

Functional Diagnosis:

Parametric Identification

The circuit under test is presented by the equations set:

$$\begin{aligned} Ax &= b \;; \\ y &= Cx \;, \end{aligned} \qquad (1)$$

where $A \in R^{n\times n}$ is nonsingular tabular matrix of n by n elements; $b \in R^{n}$ is a vector of input data, consisting from n elements; $y \in R^{m}$ is a vector of output data; $x \in R^{n}$ is a vector of internal variables, and $C \in R^{n\times n}$ is a selector matrix, which selects certain components of x for measurement (each row of C has one and only one entry being 1 and the rest of them 0), m is the number of test points, and n is the size of the system.

Functional Diagnosis:

Parametric Identification

Due to fault the matrix A is changed on ΔA and vector x on Δx or

$$\begin{aligned} (A+\Delta A)(x+\Delta x) &= b \;; \\ (y+\Delta y) &= C(x+\Delta x) \;. \end{aligned} \qquad (2)$$

Using (1) and (2), the deviation of output data y from their nominal values can be expressed as

$$\Delta y = -CA^{-1}\Delta A(x+\Delta x)\;. \qquad (3)$$

The diagnosis problem comes to receiving of values ΔA by using well known, measured values Δy.

Functional Diagnosis:

Parametric Identification

Nonlinear equation (3) can be transformed to linear form:

$$\Delta y = Mz \quad , \qquad (4)$$

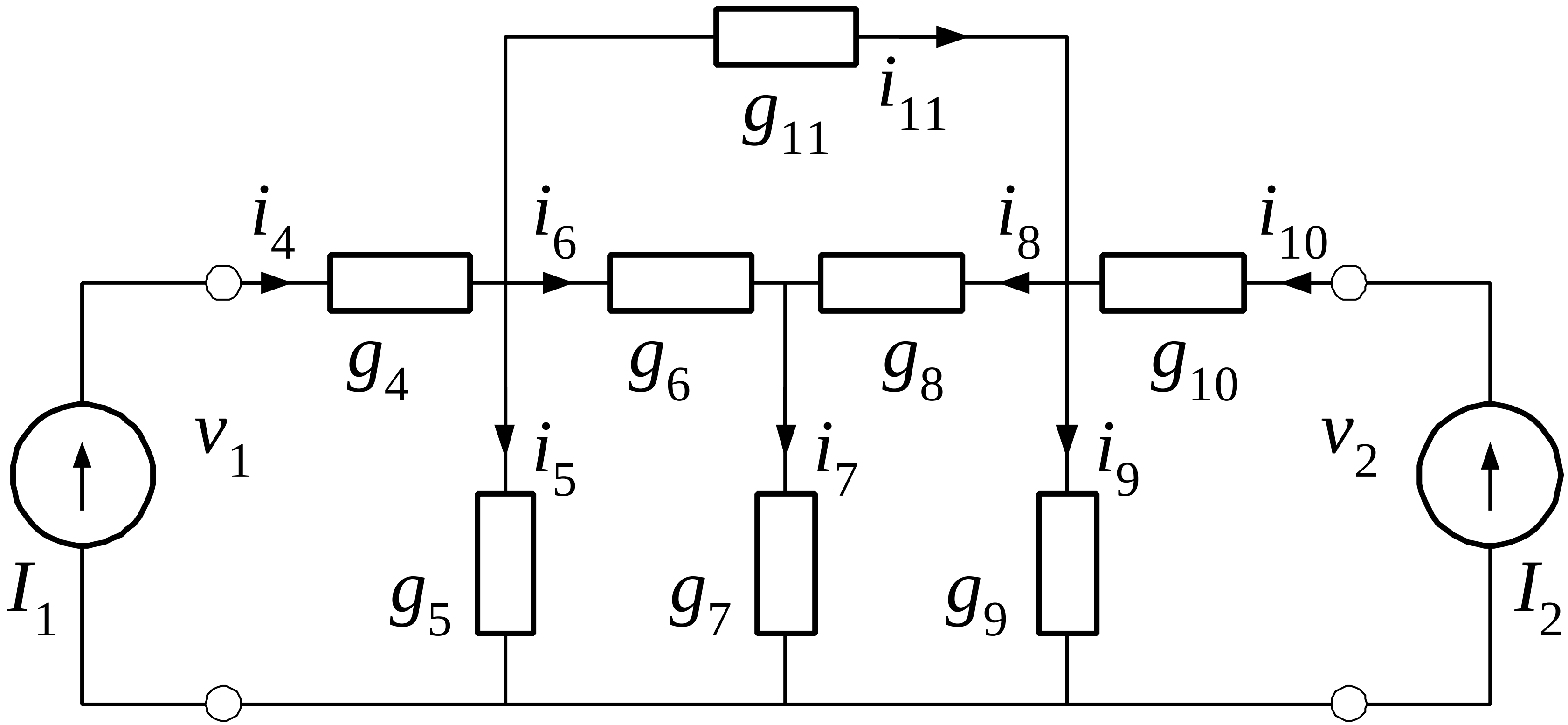
where $z \in R^n \; \left(z = \Delta A(x + \Delta x)\right)$ and $M \in R^{m \times n} \; \left(M = -CA^{-1}\right)$.

The problems of parametric identification for linear analog circuits

- The number of test nodes less than size of the system ($m << n$);
- The problem of tolerances (dA). At that case the deviation ΔA is defined by two components $\Delta A = dA_{toler} + \Delta A_{fault}$.

Functional Diagnosis:

An example of parametric identification
for linear analog circuit



Functional Diagnosis:

An example of parametric identification for linear analog circuit

The first equation from system (1) for given example is:

$$
\begin{bmatrix}
-1 & 1 & 1 & 0 & 0 & 0 & 0 & 1 & & & & & & & & & & \\
0 & 0 & -1 & 1 & -1 & 0 & 0 & 0 & & & & & & & & & & \\
0 & 0 & 0 & 0 & 1 & 1 & -1 & -1 & & & & & & & & & & \\
 & & & & & & & & -1 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
 & & & & & & & & 0 & 0 & 0 & -1 & 1 & 1 & 0 & 0 & 0 & 0 \\
 & & & & & & & & 0 & 0 & 0 & 0 & 0 & -1 & -1 & 1 & 0 & 0 \\
 & & & & & & & & 0 & 1 & 0 & 0 & 0 & 0 & 0 & -1 & -1 & 0 \\
 & & & & & & & & 0 & 0 & 0 & 0 & -1 & 0 & 1 & 0 & 0 & 1 \\
1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & & & & & & & & & & \\
0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & & & & & & & & & & \\
-1 & & & & & & & & & & g_4 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
 & -1 & & & & & & & & & 0 & g_5 & 0 & 0 & 0 & 0 & 0 & 0 \\
 & & -1 & & & & & & & & 0 & 0 & g_6 & 0 & 0 & 0 & 0 & 0 \\
 & & & -1 & & & & & & & 0 & 0 & 0 & g_7 & 0 & 0 & 0 & 0 \\
 & & & & -1 & & & & & & 0 & 0 & 0 & 0 & g_8 & 0 & 0 & 0 \\
 & & & & & -1 & & & & & 0 & 0 & 0 & 0 & 0 & g_9 & 0 & 0 \\
 & & & & & & -1 & & & & 0 & 0 & 0 & 0 & 0 & 0 & g_{10} & 0 \\
 & & & & & & & -1 & & & 0 & 0 & 0 & 0 & 0 & 0 & 0 & g_{11}
\end{bmatrix}
\cdot
\begin{bmatrix}
i_4 \\ i_5 \\ i_6 \\ i_7 \\ i_8 \\ i_9 \\ i_{10} \\ i_{11} \\ v_1 \\ v_2 \\ v_4 \\ v_5 \\ v_6 \\ v_7 \\ v_8 \\ v_9 \\ v_{10} \\ v_{11}
\end{bmatrix}
=
\begin{bmatrix}
 \\ \\ \\ \\ \\ \\ \\ \\ I_1 \\ I_2 \\ \\ \\ \\ \\ \\ \\ \\ \\
\end{bmatrix}
$$

Functional Diagnosis:

An example of parametric identification for linear analog circuit

The selector matrix *C* and second equation from system (1) for given example are:

$$\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} = C \quad \text{and} \quad y = \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = Cx$$

The equation (3) for considered example can be written as

$$\Delta y = -CA^{-1}J \quad , \tag{5}$$

where

$$J = \begin{bmatrix} J_4 \\ J_5 \\ . \\ . \\ . \\ J_{11} \end{bmatrix} = \begin{bmatrix} \Delta g_4 & & & & & \\ & \Delta g_5 & & & & \\ & & . & & & \\ & & & . & & \\ & & & & . & \\ & & & & & \Delta g_{11} \end{bmatrix} \cdot \begin{bmatrix} v_4 + \Delta v_4 \\ v_5 + \Delta v_5 \\ \\ \\ \\ v_{11} + \Delta v_{11} \end{bmatrix}.$$

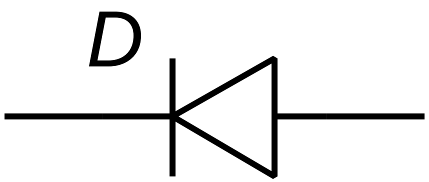
Functional Diagnosis:

The problems of parametric identification for nonlinear analog circuits

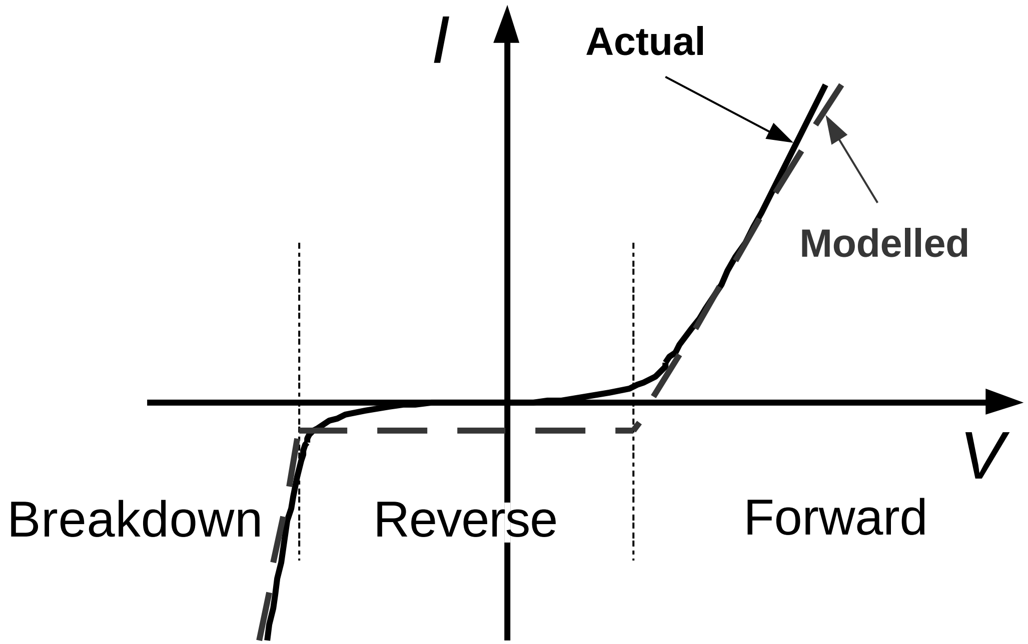
- *Biasing of active components and, as a consequence, changes of device operations mode;*
- *Multiple solution of nonlinear circuits.*

Functional Diagnosis:

Parametric identification
of nonlinear analog circuits



Diode symbolic notation



***I*-*V* (static) characteristic of diode**

Functional Diagnosis:

Parametric identification of nonlinear analog circuits

All nonlinear internal devices are replaced by models on the basis of piecewise-linear resistors. At that, circuit contains n_p two-terminal PWL resistors and all space R^{n_p} is divided into N_p number of regions by a finite number of (n_p-1)-dimentional hyperplanes. In each received region Ω_j (j = 1, 2, ..., N_p) the characteristic of each PWL resistor can be represented by affine mapping. Then the equations set for nonlinear circuit will become

$$A^{(j)}x - b^{(j)} = 0,\ x \in \Omega_j,\ j = 1,\ 2,\ \ldots,\ n_p\ ;$$

$$y = Cx \quad ,$$

where $x,\ b \in R^n;\ y \in R^m;\ A \in R^{n\times n};\ C \in R^{m\times n}$ and $\Omega \in R^n$.

Functional Diagnosis:

Parametric identification of nonlinear analog circuits

The perturbed system equation, stipulated by the deviations in operation of nonlinear device, is:

$$A^{(j)}x - b^{(j)} + \phi(x) = 0,\ x \in \Omega_j,\ j = 1,\ 2,\ \ldots,\ n_p \quad ,$$

where $\phi(x)$ is a vector of the nonlinear perturbation.

Let $x \in \Omega_j$ be a solution of the normal circuit and $\tilde{x} \in \Omega_k$ be one of the perturbed circuits. Then

$$A^{(j)}x - b^{(j)} = 0,\ x \in \Omega_j;$$

$$A^{(k)}\tilde{x} - b^{(k)} + \phi(\tilde{x}) = 0,\ \tilde{x} \in \Omega_k \quad .$$

Functional Diagnosis:

Parametric identification of nonlinear analog circuits

Usually, the normal region Ω_j is known, but the perturbed region Ω_k is unknown. The determination of Ω_k is a part of the diagnosis problem. The equations set is written in such a way that each circuit element appears in one and only one row and no two circuit elements appear in the same row. Hence, the *i-th* circuit element is perturbed if and only if the *i-th* component of vector $\phi(x)$ is nonzero.

Functional Diagnosis:

Parametric identification of nonlinear analog circuits

Using two last expressions, receive the following linear equations set

$$\left(A^{(j)} + \Delta A^{(j)}\right)\tilde{x} - \left(b^{(j)} + \Delta b^{(j)}\right) = 0 \ ,$$

where

$$\Delta A^{(j)}\tilde{x} = \left[A^{(k)} - A^{(j)}\right]\tilde{x} + \phi(\tilde{x}) \ ,$$

$$\Delta b^{(j)} = b^{(k)} - b^{(j)} .$$

The purpose of diagnosis is to identify the nonzero components of vector ϕ.

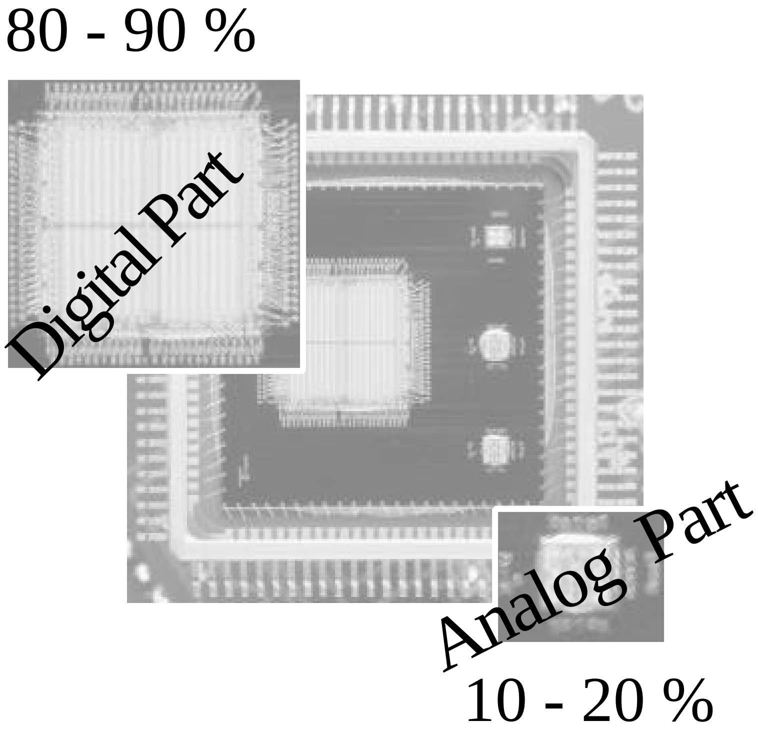
Functional Diagnosis:

Approaches of analog circuits functional diagnosis

SBT	SAT
more suitable for detection of catastrophic faults	*more suitable for detection of parametric faults*

DFT of Analog Circuits:

The features of Mixed-Signal IC development



The problems of mixed-signal circuit development:

complexity and high expenses both time and money on designing and testing of analog subcircuits

DFT of Analog Circuits:

Nayward of Design-For-Testability

Usage of design-for-testability does not allow:

- Improve the primary circuit functions;
- Make a circuit faster;
- Reduce the power consumption, etc;

Even worse:

- The chip complexity is increased;
- *DFT* strategy dominantly shapes the silicon solution;
- Increases the chip area.

DFT of Analog Circuits:

Advantages of Design-For-Testability

- Reduction of testing time and as consequence decrease of IC's total cost;
- Increasing of the fault coverage;
- Increasing of the circuit reliability;
- Verification of the output characteristics in real-time mode.

DFT of Analog Circuits:

DFT solutions for analog circuits

Reconfiguration-based test	**Code-based test**
• Division on functional blocks; • Rearranging of circuit internal structure.	The methods of Code-based approach are used for on-line testing and allow to decide task of measuring the values of on-chip signals in real time mode. A redundant data code is used to encode on-chip data.

DFT of Analog Circuits:

The groups of DFT techniques for analog circuits

- *Support for External Test and Evaluation;*
- *Access to Embedded Blocks;*
- *On-chip Test Evaluation;*
- *Built-In Self-Test;*
- *On-chip Multi-Module System Test.*

DFT of Analog Circuits:

Support for External Test and Evaluation

- *I_{DDQ} testing;*
- *Transient Response Testing;*
- *Residual Multiple Frequency Testing.*

DFT of Analog Circuits:

Comparative appraisal of on-chip and off-chip tests of analog ICs

Feature	On-chip test	Off-chip test
Speed of execution	high (+)	low (-)
Additional chip area	needed (-)	not needed (+)
Operating mode	on-line and off-line (+)	only off-line (-)
Requirements to used test equipment	standard (universal) (+)	specialized, expensive (-)
Accuracy	high (+)	low (-)
Implementation cost	high (-)	low (+)

DFT of Analog Circuits:

Multifrequency testing

Limitations and Requirements made to a product:

- *The limited number of external outputs;*
- *Power consumption;*
- *Geometrical sizes, etc.*

The number of test nodes n_n is essential less the number of possible faults n_f, $n_n << n_f$.

DFT of Analog Circuits:

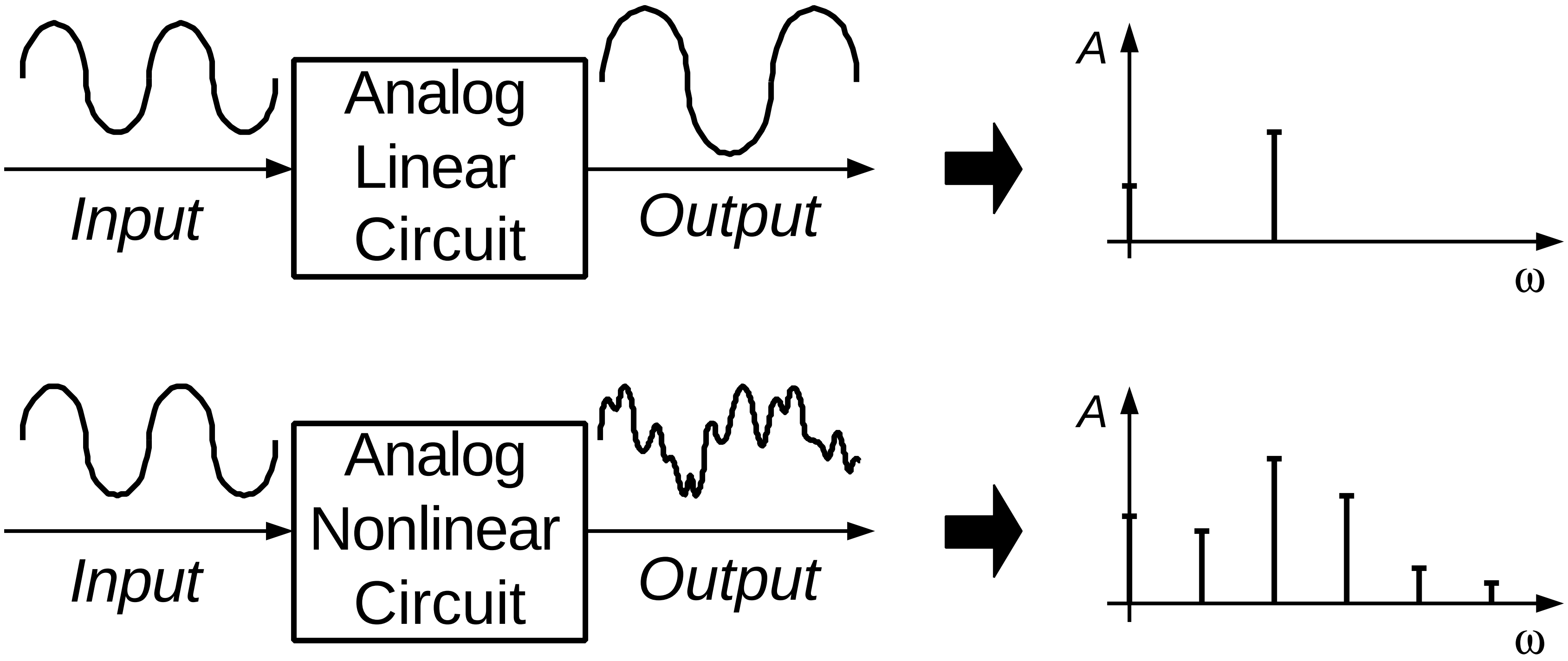
Multifrequency testing

Usage of a sine wave signal of variable frequency and amplitude as excited test signal allows:

- To receive a family of output responses at each test nodes.
- To choose the optimal frequencies which enable to reduce number of applied test signals and used output nodes.

DFT of Analog Circuits:

Multifrequency testing



The features of sine wave usage for linear and non-linear circuits

DFT of Analog Circuits:

Multifrequency testing and Sensitivity analysis

The deviation of circuit function $y(x_1, x_2, ..., x_i,..., x_N)$ can be expressed by Taylor's series as follows

$$y(x_1,...,x_i,...,x_N) - y(x_{10},...,x_{i0},...,x_{N0}) = \frac{\partial y}{\partial x_1}(x_1 - x_{10}) + ... + \frac{\partial y}{\partial x_i}(x_i - x_{i0}) + ... +$$

$$+ \frac{\partial y}{\partial x_N}(x_N - x_{N0}) + \frac{1}{2!}\sum_{i=1}^{N}\sum_{j=1}^{N}\frac{\partial^2 y}{\partial x_i \partial x_j}(x_i - x_{i0})(x_j - x_{j0}) + Rm(x_1,...,x_i,...,x_N)$$

or in the differential form as

$$y(x_{10} + dx_1,...,x_{i0} + dx_i,...,x_{N0} + dx_N) - y(x_{10},...,x_{i0},...,x_{N0}) =$$

$$dy + \frac{1}{2!}d^2 y + ... + \frac{1}{(m-1)!}d^{m-1}y + Rm \; .$$

DFT of Analog Circuits:

Multifrequency testing and Sensitivity analysis

Total increment of circuit function:

$$\Delta y = \frac{\partial y}{\partial x_1}\left(x_1 - x_{10}\right) + \ldots + \frac{\partial y}{\partial x_i}\left(x_i - x_{i0}\right) + \ldots + \frac{\partial y}{\partial x_N}\left(x_N - x_{N0}\right)$$

where $(x_i - x_{i0}) = \Delta x_i$ is deviation of circuit component parameter x_i from its nominal value, or

$$\Delta y = \sum_{i=1}^{N} S_i \Delta x_i$$

where $S_i = \frac{\partial y}{\partial x_i}$ is absolute sensitivity of circuit output function y to deviation of circuit component parameter x_i.

DFT of Analog Circuits:

Multifrequency testing and Sensitivity analysis

For deviations of the output characteristics in all available test nodes at various input signals, the following system is formed

$$\Delta Y = S_X^Y \Delta X \quad ,$$

where ΔY is the vector of output characteristic deviations;
ΔX is the vector of circuit components parameters deviations;
S_X^Y is the matrix of sensitivity functions.

Component x_i $\left(\forall i,\ i \in [1..N]\right)$, value Δx_i of which exceeds tolerable limit, is considered faulty.
The ***sensitivity*** can be considered as ***observability*** of internal component x under the output characteristic y.

DFT of Analog Circuits:

The methods of the Sensitivity calculation:

- *Method of the circuits in increments;*
- *Indirect methods of definition;*
- *Method of sensitivity models;*
- *Method of the adjoint circuit, etc.*

DFT of Analog Circuits:

The method of Adjoint Circuit

The application of adjoint circuit method under single calculation of two circuits (original and attached) allows to compute the sensitivity coefficients of one output function *F* with respect to all internal parameters of the circuit x_i.

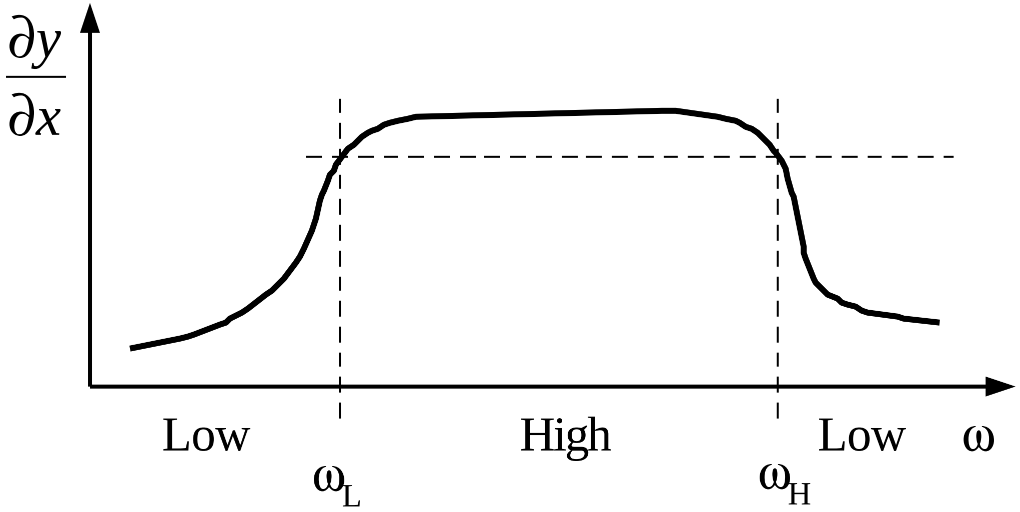
Element	Original Circuit	Adjoint Circuit	Sensitivity
Resistor, R	$U_R = RI_R$	$\tilde{U}_R = R\tilde{I}_R$	$-I_R\tilde{I}_R$
Conductance, G	$I_G = GU_G$	$\tilde{I}_G = G\tilde{U}_G$	$-U_R\tilde{U}_R$
Inductance, L	$U_L = j\omega LI_L$	$\tilde{U}_L = j\omega L\tilde{I}_L$	$-j\omega I_L\tilde{I}_L$
Capacitor, C	$I_C = j\omega CU_C$	$\tilde{I}_C = j\omega C\tilde{U}_C$	$-j\omega U_C\tilde{U}_C$

$$\frac{\partial|F|}{\partial x} = |F| * \mathrm{Re}\left(\frac{\partial F}{\partial x} * \frac{1}{F}\right)$$

$$\frac{\partial(\arg F)}{\partial x} = \mathrm{Im}\left(\frac{\partial F}{\partial x} * \frac{1}{F}\right) * \frac{180}{\pi}$$

DFT of Analog Circuits:

Multifrequency testing and Sensitivity analysis



Test vector $\Omega = [\omega_1, \omega_2, \ldots, \omega_N]$ ($\omega_L < \omega_i < \omega_H \ \forall i \left(i \in [1..N]\right)$) is optimal if the number of test frequencies N is minimum and frequencies $\omega_i \ \forall i \left(i \in [1..N]\right)$ allow to detect a maximum of faults.

Output node n_i is a test node ($n_i \in TN$, TN is the set of test nodes) if

$$S_x^{y_{n_i}} \neq S_x^{y_{n_j}} \text{ for } \forall\left(n_i, n_j\right), i \neq j .$$

DFT of Analog Circuits:

Multifrequency testing and Sensitivity analysis

The searching of a minimum coverage at minimum number of used test nodes will allow to generate the compact fault dictionary with optimal structure.

Circuit output characteristic used for testing

↙ ↘

Amplitude or Gain of output voltage in test nodes

Phase function of output voltage in test nodes

DFT of Analog Circuits:

The Algorithm of Multifrequency testing using Sensitivity analysis

1. Compute frequency response function for gain and phase.
2. Define a set of circuit nodes, from which in future the test nodes will be selected.
3. Define the set of possible faults.
4. Calculation of sensitivity function value for the amplitude and phase of voltage.
5. Searching of a minimum coverage of faults set by set of output responses. The choice of test nodes and test vector.
6. Construction of the fault dictionary.

Built-In Self-Test:

The strategies of Built-In Testing

On-line (working mode)	Off-line (dedicated mode)
Faults are detected during execution by the circuit of intended for it function	Tested circuit is switched to the dedicated mode, at which the usual operation of the device is impossible

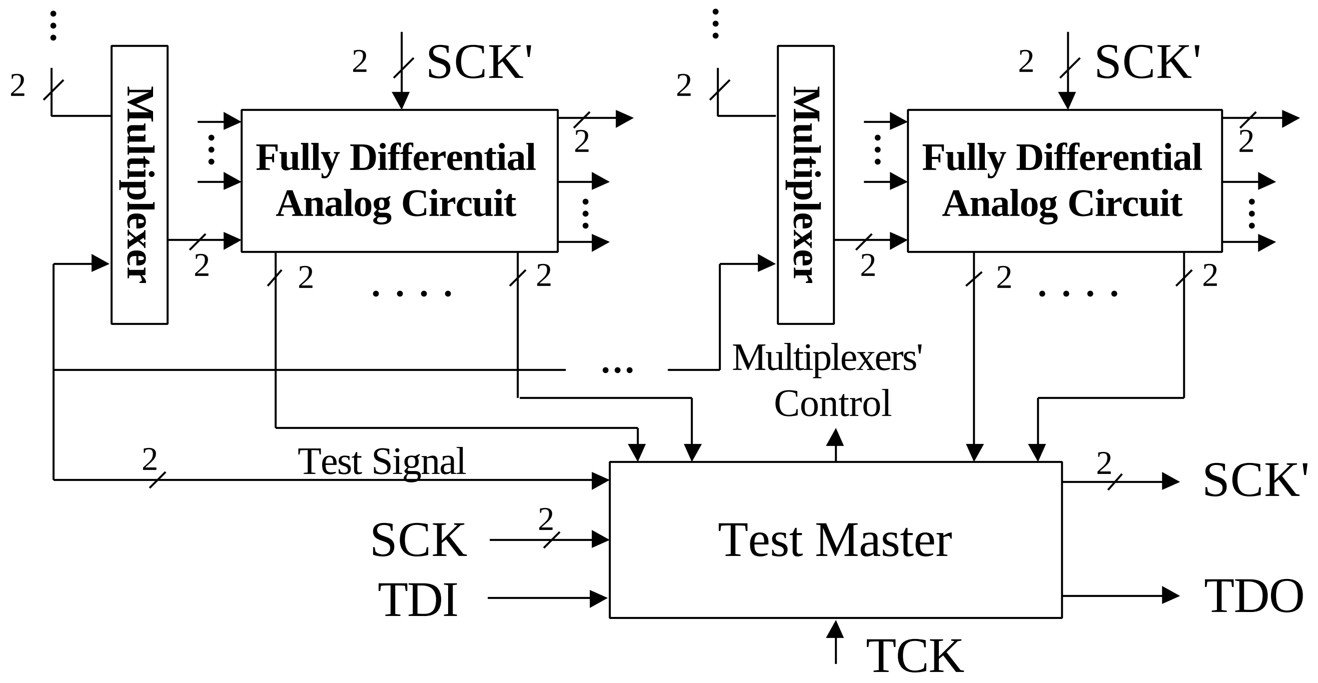
Built-In Self-Test:

The differences between BIST solutions

- Ways of input test signal selection;
- Ways of output responses processing;
- Choice of controlled (measured) parameters;
- Modes of operation;
- Classes of tested devices.

Built-In Self-Test:

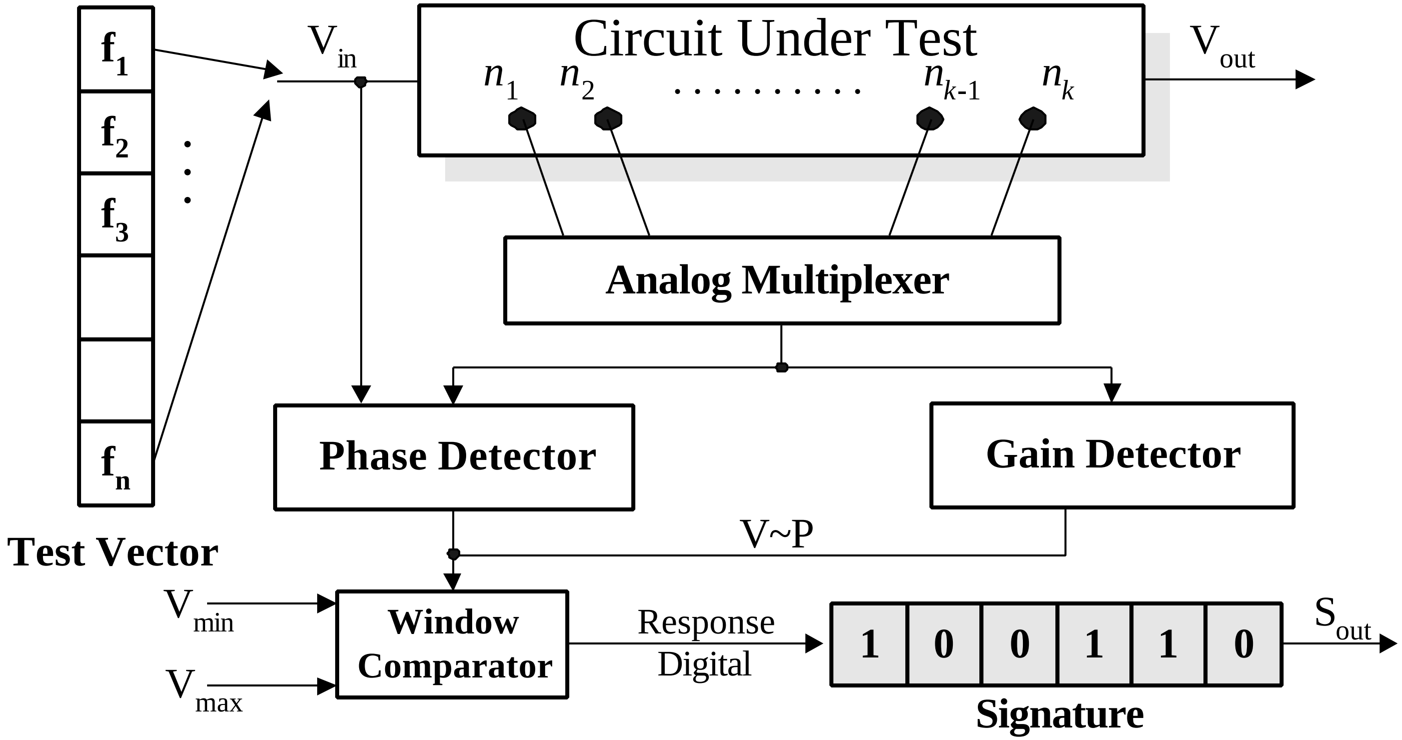
Analog Unified BIST (AUBIST) *



* - was proposed at the works of authors S. Mir, M. Libaszewski, V. Colarik and B. Courtois

Built-In Self-Test:

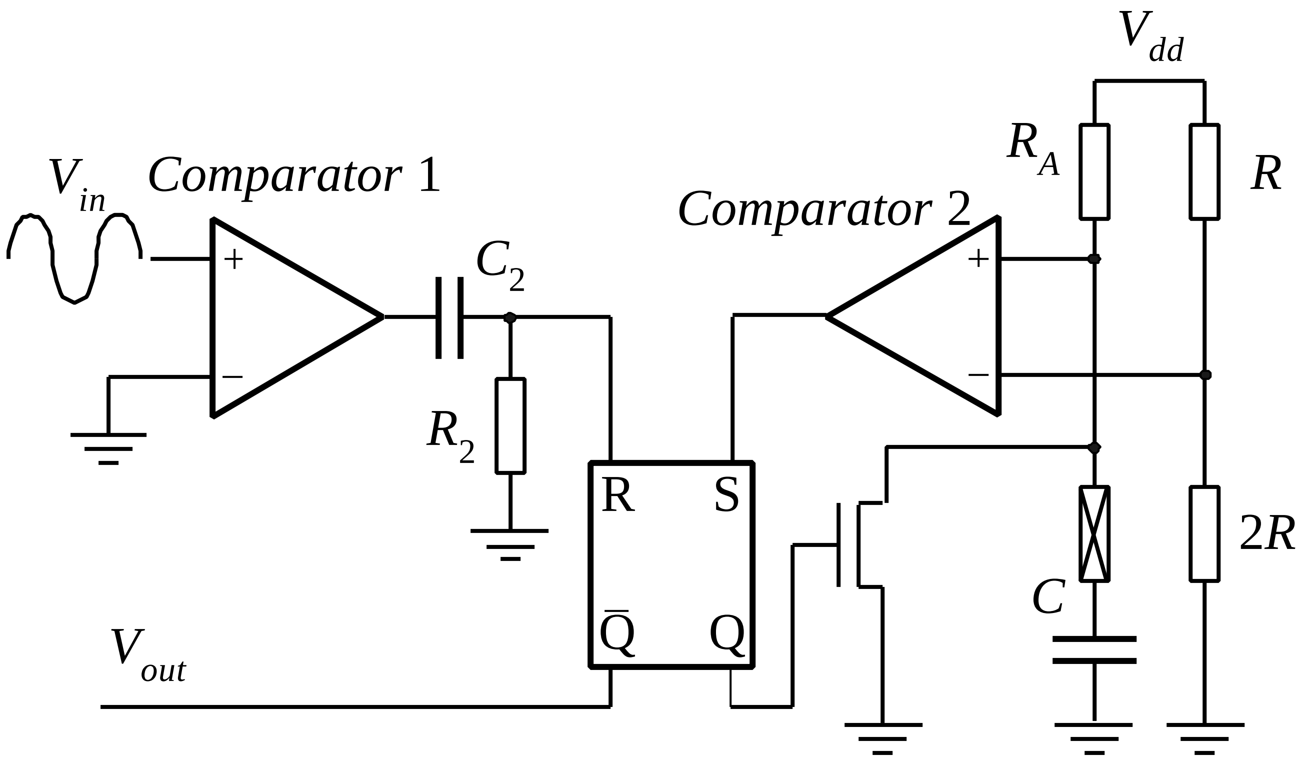
Translation BIST (T-BIST) *



* - was proposed at the works of authors M. Slamani, B. Kaminska and G. Quesnel

Built-In Self-Test:

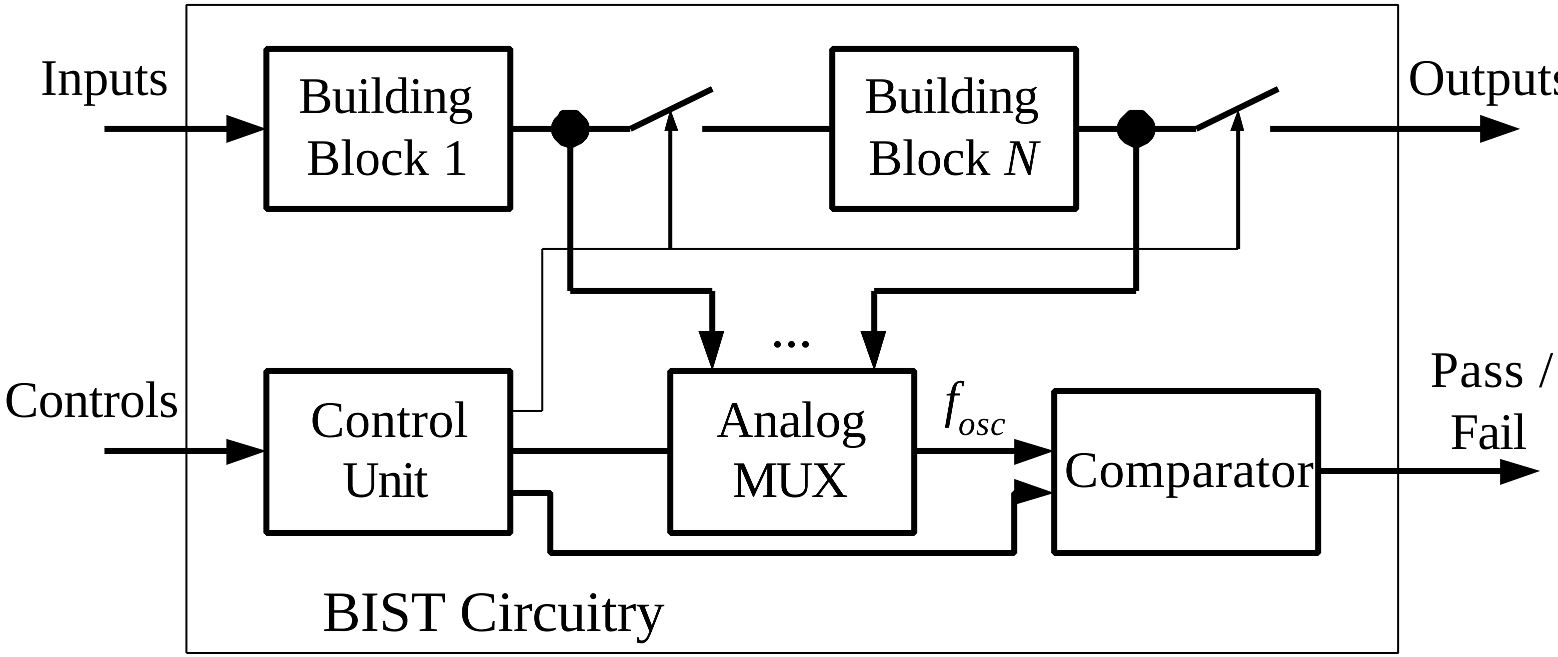
Frequency-based BIST (f-BIST) *



* - was proposed at the works of authors S. Khaled, B. Kaminska, B. Courtois and M. Lubaszewski

Built-In Self-Test:

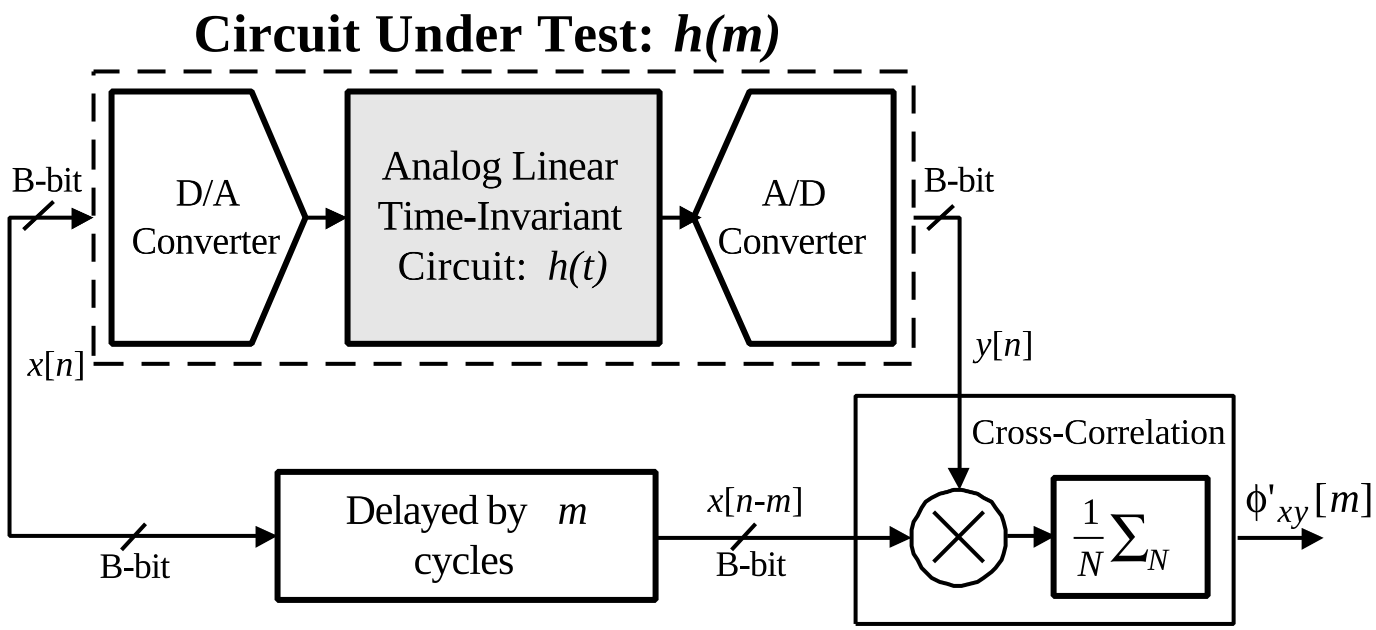
Oscillation BIST (OBIST) *



* - was proposed at the works of authors K. Arabi and B. Kaminska

Built-In Self-Test:

Implicit Functional Testing *



$\phi_{xy}[m] = \sigma_x * h[m]$, when $x[n]$ is a white noise with mean μ_x=0 and standard deviation σ_x.

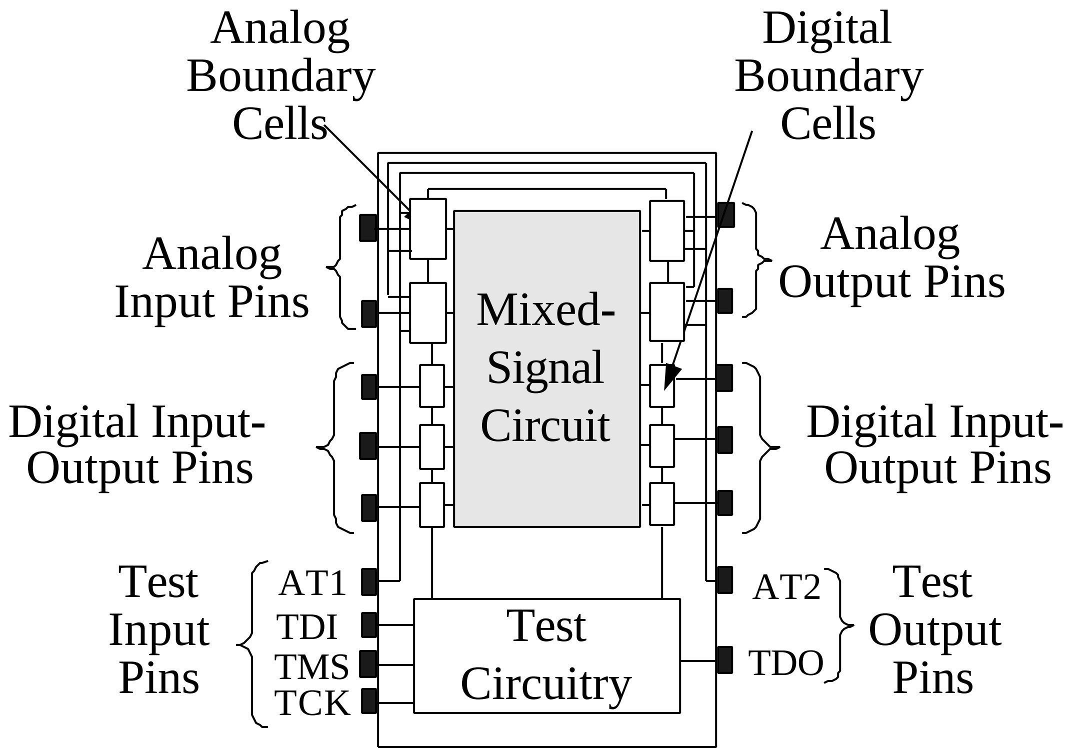
In practice, only finite number N of samples is used to estimate the signatures:

$$\phi'_{xy}[m] = \frac{1}{N}\sum_{n=0}^{N-1} x[n-m] * y[n]$$

* - was proposed at the works of authors Chen-Yang Pan and Kwang-Ting Cheng

Analog-digital test bus:

Architecrure of IEEE 1149.4 mixed-signal test bus



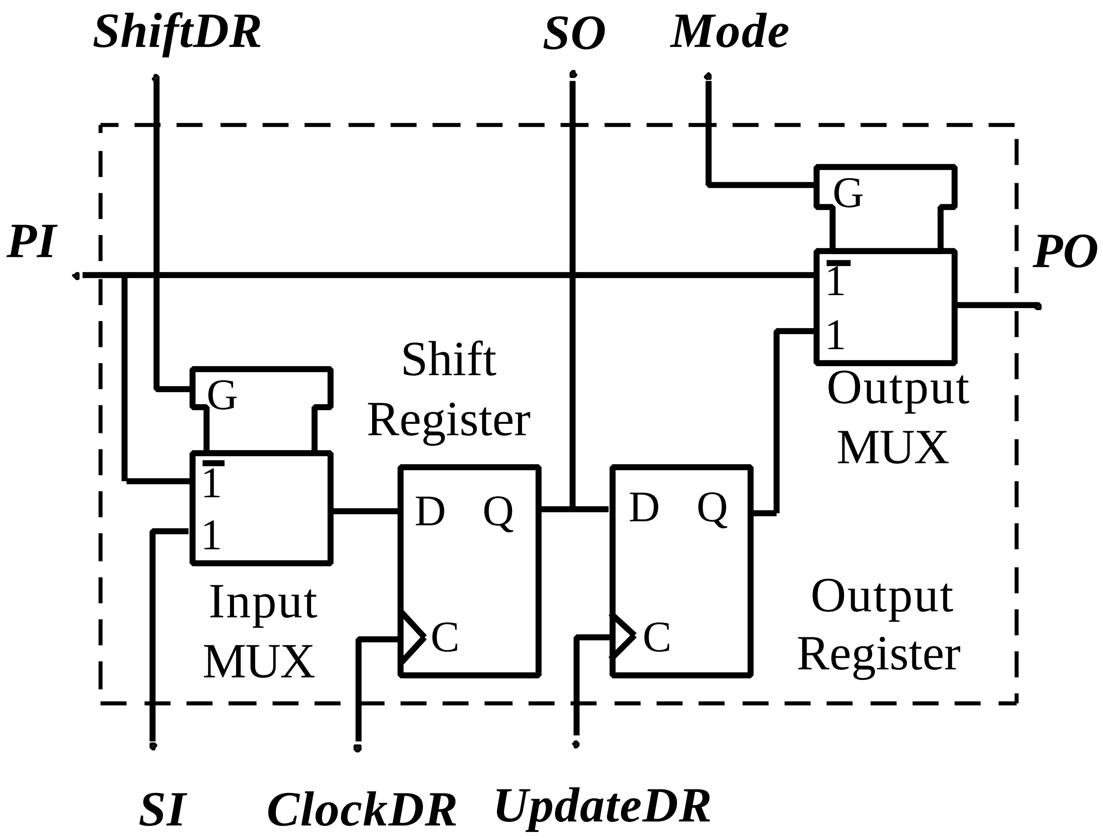
Analog-digital test bus:

IEEE 1149.4 standard provides
the following test outputs

- **TDI** (Test Data In) - sequential input of test data;
- **TDO** (Test Data Out) - three-stable sequential output of test data;
- **TMS** (Test Mode Select) - signal of a test mode choice;
- **TCK** (Test Synchronizing Clock) - signal of test logic synchronization, is independent from system's synchronizing signal;
- **AT1** and **AT2** - signals of analog subcircuit testing.

Analog-digital test bus:

Structure of Digital Boundary Scan Cell



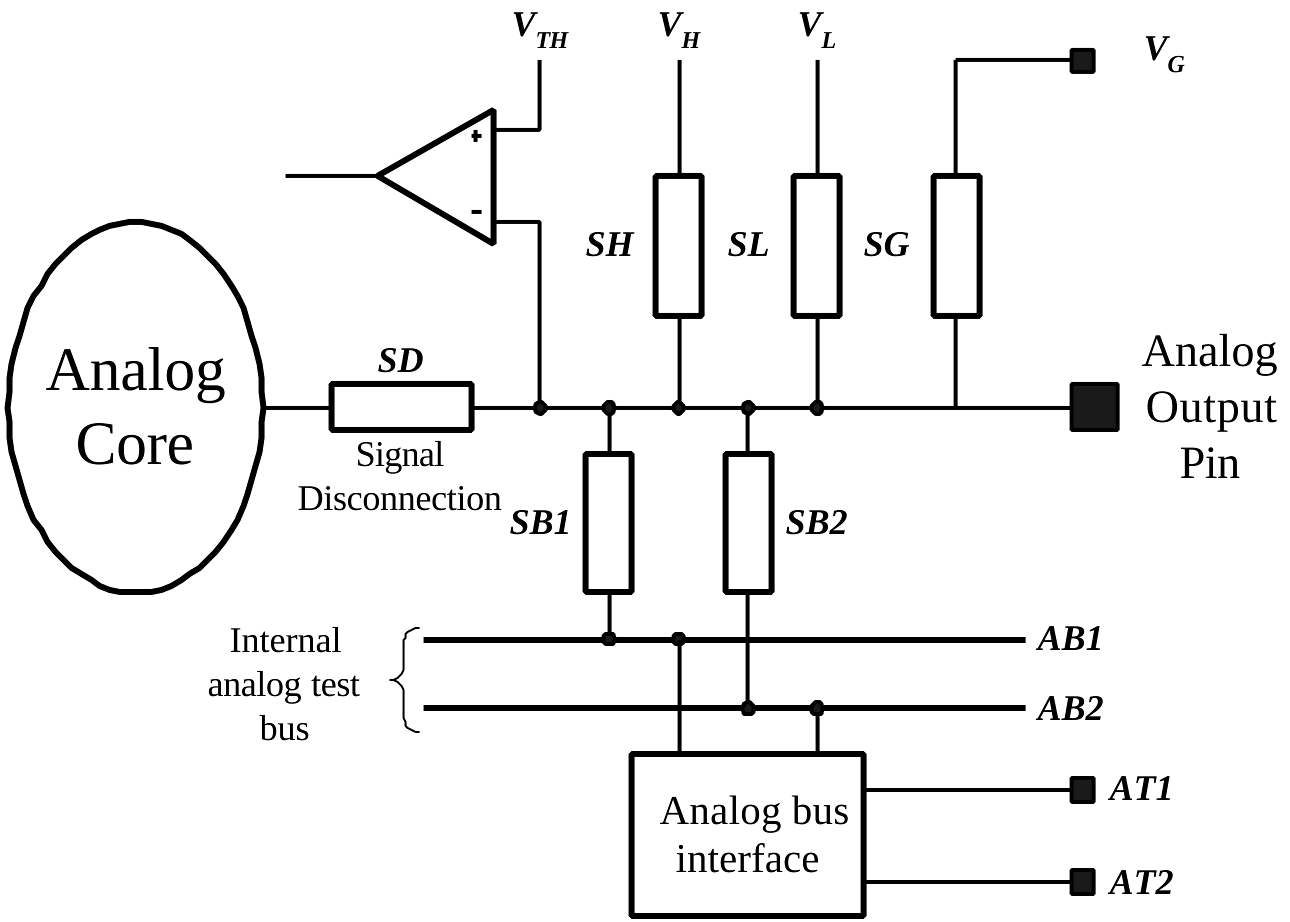
Analog-digital test bus:

The modes of the BSC operation

- **Normal mode**, at which the data pass directly from an input *PI* straight to an output *PO*.
- **Upgrade mode**, at which the data of the output register is passed through to an output *PO*;
- **Capture mode**, at which the data from an input *PI* move to the shift register, and the value is captured by the next ClockDR;
- **Shift mode**, at which the data are transferred from an output *SO* (Scan Out) of one cell to an input *SI* (Scan In) of the next cell.

Analog-digital test bus:

Structure of Analog Boundary Module



Analog-digital test bus:

The functions of Analog Boundary Module

- Disconnect the Input-Output pin from the analog core;
- Set the Input-Output pin at a logic high or low level;
- Detect the logic level present on the Input-Output pin;
- Connect the Input-Output pin to a two-wire analog test bus.

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